

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/Backlog), Dec 2023

BCA, Semester I

Roll No.....

CS1117: Computer Organisation and Systems

Time: 2 hours

Max. Marks: 30

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

Q.1	Convert the following as instructed: a) $(625)_8$ to Hexadecimal b) $(FFB)_{16}$ to Decimal.	03 (CO9)
Q.2	Minimize the given function using Karnaugh Map. $F(A, B, C, D) = \sum m(0, 2, 8, 10, 14) + \sum d(5, 15)$	03 (CO2)
Q.3	Write the following -121.25 in single precision IEEE representation	03 (CO5)
Q.4	Multiply 21 with -21 using Binary representation of numbers. (show the working steps)	03 (CO2)
Q.5	Write the control signals using single bus CPU organization for instruction. Add A, [A], B ; Add the contents of Register B to the contents of location pointed by Register A and Store the result in the Register A.	03 (CO1)
Q.6	Consider a Pipeline with 4 stages S1, S2, S3, S4 with execution times 1ms, 2ms, 1ms, 2ms. Consider four instructions I1, I2, I3, I4 which use these stages as following: I1: S1 S3 S4 I2 : S1 S2 S3 S4 I3 : S1 S2 S4	04 (CO6)

	I4 : S1, S2, S3 a) Calculate the total time taken to execute these instructions serially (in order I1, I2, I3, I4) if there was no pipelining. b) Calculate the total time taken for a) with the pipelining. Draw the Time-space diagram for the execution of 4 instructions. Assume that there is no data dependency among the instructions. (Hint: consider structural hazards)	
Q.7	For each statement below, indicate if it is true or false. Each correct reply gives you 0.5 mark. a) ROM is volatile. b) SRAM needs periodic refreshing. c) Microprogrammed control is faster than Hardwired control. d) There are two representations of 0 in 2's complement representation of an integer. e) Shortest Seek Time algorithm may lead to starvation. f) Any Memory block can be stored in any Cache block in Set Associative Cache organization. g) Some interrupts can not be masked. h) RAM is volatile	04 (CO1 to CO9)
Q.8	Consider the main memory have three cache blocks (0,1,2) and fully associative cache memory architecture. Processor requires the pages from the in the following order 6, 7,8,7,9,7,8,9, 8, 9, 1. Show the implementation of FIFO. Also calculate Hit ratio.	04 (CO7, CO8)
Q.9	Explain ROR, AND, ADD instruction using suitable example.	03 (CO3)