

JK Lakshmipat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Backlog), May 2019
B. Tech. in Computer Science and Engineering, Semester IV

Roll No.....

CSE403: COMPUTER ARCHITECTURE AND ORGANIZATION

Time: 03 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A	Objective type multiple choice questions (10 questions @ 1 mark)	10
i.	The communication between central system and the outside environment is done by A) Input-output subsystem B) Control system C) Memory system D) Logic system	
ii.	Cache memory works on the principle of (A) Locality of data. (B) Locality of reference (C) Locality of memory (D) Locality of reference & memory	
iii.	Program always deals with A). Logical address B). absolute address C). Physical address D). Relative address	
iv.	In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is A). Before effective address calculation has started B). During effective address calculation C). After effective address calculation has completed D). After data cache lookup has completed	
v.	Memory unit accessed by content is called_____. A). Read only memory B). Programmable Memory	

	C). Virtual Memory	D). Associative Memory	
vi.	Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called A). Fragmentation B). Paging C). Mapping D). None of the mentioned		
vii.	SIMD represents an organization that _____. A). Refers to a computer system capable of processing several programs at the same time. B). Represents organization of single computer containing a control unit, processor unit and a memory unit. C). Includes many processing units under the supervision of a common control unit D). None of the above.		
viii.	The branch logic that provides decision making capabilities in the control unit is known as A). Controlled transfer B). Conditional transfer C). Unconditional transfer D). None of above		
ix.	Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus? A. 1 Megabyte/sec B. 4 Megabytes/sec C. 8 Megabytes/sec D. 2 Megabytes/sec		
x.	Which of the following are true for memory interleaving? a. The lower order address lines are connected to the address lines of the memory chips. b. Consecutive memory addresses are mapped to consecutive memory modules. c. Permits faster data transfer for word-aligned data. d. None of the above		
Q.2	Short answer type questions (4 questions @ 2.5 marks)		10
i.	What is Instruction Level Parallelism?		
ii.	What is the difference between logical, circular and arithmetic shift?		
iii.	Why Read and Write lines of a DMA controller are bi-directional?		
iv.	What is a port? Differentiate between serial and parallel port?		
Q.3A	What are different types of bus interfaces? Explain in detail USB bus organization.		05
Q.3B	Identify the dependencies in the following code: I1: R1 ← R6 + 100 I2: R5 ← R1 + R2		05

I3: $R7 \leftarrow R5 + 1$
 I4: $R1 \leftarrow R2 + R4$
 I5: $R5 \leftarrow R6 + 22$
 I6: $R2 \leftarrow R4 - 25$
 I7: $R3 \leftarrow R7 - 2$
 I8: $R4 \leftarrow R1 + R3$
 I9: $R10 \leftarrow R6 - 100$
 I10: $R1 \leftarrow R1 + 30$

- I). Identify the RAW, WAR, and WAW dependencies of the above instruction?
- II). Remove dependencies by providing stalls?
- III). Rename the registers in the above sequence to prevent, where possible, dependency problems.

Q.4A	Discuss Page replacement policies. Consider the following reference string and determine the number of page faults using given algorithms- 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5, 2, 3, 1, 5 A. LRU B. FIFO C. Optimal	05
Q.4B	Differentiate desktop, Server & embedded computing classes based on their 3 system characteristics?	05
Q.5A	What is cache coherency and how is it eliminated?	05
Q.5B	Draw the memory hierarchy system. Clearly mention the speed, capacity and access type at each level of memory hierarchy OR	05
Q.5B	How can you justify Daisy Chain priority is useful in priority interrupt?	05
Q.6A	Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. What will be the capacity of the disk pack and the number of bits required to specify a particular sector in the disk ?	05
Q.6B	What is parallel processing and what are the different levels of parallel processing? How parallelism can be achieved in uni-processor system?	05
Q.7A	Assume a disk subsystem with the following components and MTTF: o 10 disks, each rated at 1,000,000 hour MTTF o 1 SCSI controller, 500,000 hour MTTF o 1 power supply, 200,000 hour MTTF o 1 fan, 200,000 hour MTTF	05

o 1 SCSI cable, 1,000,000 hour MTTF

Using the assumptions that the lifetimes are exponentially distributed and that failure are independent; compute the MTTF of the system as a whole.

Q.7B	Explain in detail RISC pipeline. Why is the cache miss penalty, greater in deeply pipelined processor?	05
Q.8A	Why do we need I/O interface? How does I/O Bus communicate to I/O devices? What are the different ways in which computer buses can be used to communicate with memory and I/O?	10
Q.8B	Discuss associative mapping technique and state its advantages over direct mapping technique?	05
OR		
Q.8B	Differentiate between serial synchronous and serial asynchronous modes of data transfer. Explain in brief simplex and duplex modes.	05
Q.9A	Consider you have 512×8 ROM chips to build a main memory bank. I). How many of these chips are needed to provide a memory capacity of 1024 MB? II). How many lines of the address bus must be used to access 256MB of memory (one byte at a time)? How many of these lines will be common to all the chips? III). How many lines must be decoded in order to select the right chip (activate chip select)?	10
Q.9B	What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt?	05
OR		
Q.9B	Define Spec ratio. Show that the ratio of the geometric means is equal to the geometric mean of the performance ratios, & that the reference computer of SPEC ratio matters not.	05