

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Retest), February 2022

BCA, Semester I

Roll No.....

CS1117: Computer Organisation and Systems

Time: 3 hours

Max. Marks: 60

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

Q.1A	Design the JK Flip Flop using SR Flip Flop.	04
Q.1B	Consider a non-pipelined processor with a clock rate of 3.5 gigahertz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with four stages but due to the internal pipeline delay, the clock speed is reduced to 3 gigahertzes. Assume there are no stalls in the pipeline. Calculate the following i. Cycle Time in Non-Pipelined Processor ii. Non-Pipeline Execution Time iii. Cycle Time in Pipelined Processor iv. Pipeline Execution Time v. Speed Up Ratio	06
Q.2	Write and illustrate an 8086 assembly program to subtract two 16-bit numbers, FFE3 (Hexadecimal) and F0A0 (Hexadecimal). Store the result at 3006 and 3008 memory address.	10
Q.3	The access time of a cache memory is 600 ns and that of main memory 700 ns. It is estimated that 60 percent of the memory requests are for read and the remaining 40 percent for write. The hit ratio for read access only is 0.7. i. What is the average access time of the system considering only memory read cycle? ii. What is the average access time of the system for both read and write cycle? iii. What is the hit ratio taken into consideration the write cycles?	10

Q.4A	Explain the FIFO algorithm of page replacement in virtual memory concept using suitable diagram and example.	04
Q.4B	Explain the concept of memory interleaving with suitable example. Implement it using lower order interleaving method.	06
Q.5	A block-set associative cache memory consists of 128 blocks divided into four block sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words. - How many bits are required for addressing the main memory? - How many bits are needed to represent the TAG, SET and WORD fields?	10
Q.6A	Differentiate between different type of interrupts used in 8086.	05
Q.6B	The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 58,308 kilobytes from disk to main memory. The memory is byte addressable. Calculate the minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory.	05