

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination, May 2022
B. Tech. (ECE), Semester IV, 2020-22

Roll No.....

EE1110: Digital Systems Design

Time: 2 hours

Max. Marks: 30

OPEN BOOK/OPEN NOTES

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Mention all the assumptions for your answers clearly.

Q1. (a) Design a 4:1 Multiplexer using any HDL using any two programming architectures [LO2]

5M

Q1 (b) Compare the programming architectures used stating the benefits/ limitations in tabular form.

[LO1]

5M

Q2 (a). Explain the applications of any one type of Shift register.

[LO2]

5 M

(b) Write the HDL program to implement the schematic designed in 2(a).

[LO3]

5 M

Q3 (a) The VDL code for FSM of Automatic Washing machine control panel is shown below, Draw the FSM diagram for this implementation.

[LO5]

5 M

Current State	Start	Water	Timer	Next State
Idle	1	0	0	Rinse
Rinse	1	1	0	Rinse
Rinse	1	1	1	Wash
Wash	1	1	1	Dry
Dry	0	0	1	Idle
Current State	Inputs		Outputs	

	Start	Buzzer
Idle	1	0
Dry	0	1

Q1 (b) Write VHDL/Verilog code to implement the FSM of the washing machine

[LO5]

5 M

all the best!