

JK Lakshmipat University, Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination, November 2025

B. Tech, Semester-III

Roll No.....

Course Code: CS1134

Time: 2.5 Hours Total Marks – 30

Course Name: Computer Organization and Architecture

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Calculators are allowed

Q 1	A. The two's complement integer division algorithm described conventionally is known as the restoring method because the value in the A register must be restored following unsuccessful subtraction. A slightly more complex approach, known as non-restoring, avoids unnecessary subtraction and addition. Propose an algorithm for this latter approach. Use a flowchart to explain it. B. The following numbers use the IEEE 32-bit floating-point format. What is the equivalent decimal value? Use the bias value used for IEEE 32-bit format. a. 1 10000011 1100000000000000000000 b. 0 01111110 1010000000000000000000	03 03 CO 2
Q 2	A. In case of scaled direct register indexed addressing, effective address of operand is calculated as <i>displacement + contents of a base register + contents of index register * scaling factor</i>. Using the above method calculate the effective address for the following instructions. a. mov al,8[ebx][esi*4] b. mov al,1000h[esi*8] ebx contains 1000h and esi contains 4 (all addresses used are in Hexadecimal mode). B. Which statements are True for RISC architectures: (i) Primary goal is to speedup individual instruction (ii) Small Code Sizes (iii) Multiple-clock instructions (iv) "LOAD" and "STORE" are independent instructions (v) Easy to apply pipelining. Explain each option you select with brief reasons.	03 03 CO 3 CO 5

Q3	A. A computer has a cache, main memory and a disk used for virtual memory. An access to the cache takes 10 ns. An access to main memory takes 100 ns. An access to the disk takes 10,000 ns. Suppose the cache hit ratio is 0.9 and the main memory hit ratio is 0.8. The effective access time required to access a referenced word on the system is _____ when- a. Simultaneous access memory organization is used. b. Hierarchical access memory organization is used. B. Consider a direct mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order- 3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24 Which of the following memory blocks will not be in the cache at the end of the sequence? 1.3 2.18 3.20 4.30	03 03 CO 4
Q4	A. Define the technique called branch prediction to handle control hazards in pipelining.? Where and how is it used? Explain with examples. B. Consider a program with only 4 instructions in a loop repeated 2 times Repeat 2 times: I1, I2, I3, I4 We are using a pipeline processor with 4 stages S1, S2, S3, S4. Time taken (in cycles) in these stages for instructions are I1: 1,2,2,1; I2: 1, 1, 1, 1; I3: 2,1,1,1; I4: 1,2,1,2. Draw the space time diagram for execution for the program and calculate the number of cycles needed for execution of the program. Assume that there is no data dependence among the instructions.	03 03 CO 5
Q5	A. Write an ALP of subtraction of two unsigned numbers. Also explain following cases in detail with impact on Carry Flag. AE (h) – 8F (h) 8D (h) – AF (h) B. If you have 16 bit number in register AX. Write an arithmetic instruction to clear the lower 8 bits of AX. C. Explain ROL and SHL instruction in detail with an example.	03 01 02 CO 3