

**JK Lakshmipat University Jaipur**  
**INSTITUTE OF ENGINEERING AND TECHNOLOGY**

End Term Examination, December 2025  
 B. Tech. (ECE), Semester VII / B.Tech. (CCE), Semester V 2025-26

Roll No.....

CS1252: Digital System Design Using HDL

Time: 2:30 hours    Max. Marks: 40

- Do not write anything other than your roll number on question paper.
- Mention all the assumptions for your answers clearly.
- The student, before starting to write the solutions, should please check the question paper for any discrepancy and ensure that they have delivered the question paper of right course code.
- Total 8 Questions are there.

|     |   |                                                                                                                                                                                                                                                                               |             |
|-----|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Q 1 |   | Let x1, x2 and x3 are the three switches used to control a single lamp "F". Light will be ON, if exactly one switch or three switches are closed and it will be OFF, if two or no switches are closed. Design a logic circuit along with a truth table and logical expression | 5<br>(CO 3) |
| Q 2 |   | How would you design a 4 x 16 decoder using 3 x 8 decoder. Explain each step of your design approach.                                                                                                                                                                         | 3<br>(CO 3) |
| Q 3 | a | Design 2 bit Up/Down Counter and explain its working.                                                                                                                                                                                                                         | 4<br>(CO 3) |
|     | b | Design a Asynchronous with <b>active low reset</b> and synchronous with <b>active high reset</b> D FF in Verilog HDL and draw the expected output waveform. Mention comments for each Verilog command.                                                                        | 4<br>(CO 4) |
| Q 4 | a | Design a logic circuit such that output Y is equal to complement of C when A=B, and output Y is same as C when A and B inputs are different. Implement the simplified expression using Verilog HDL.                                                                           | 4<br>(CO 4) |
|     | b | Develop a system that outputs a '1' when the input sequence "101" is detected in a continuous stream of 0s and 1s. Otherwise, the output should be '0'. Non overlapping.                                                                                                      | 4<br>(CO 5) |

|    |   |                                                                                                                                                                                                                                                     |             |
|----|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Q5 | a | Realize NMOS complex logic gates using the Boolean function $Z=A(D+C)+BE$                                                                                                                                                                           | 3<br>(CO 2) |
|    | b | Compare in terms of Performance Power and Area (PPA) matrix CMOS logic Inverter and Pseudo NMOS Logic inverter.                                                                                                                                     | 4<br>(CO 1) |
| Q6 |   | Given an CMOS inverter with the following parameters: $V_{DD} = 3V$ , $V_{tn} = 0.6V$ , $V_{tp} = -0.82V$ , $k'_n = 100\mu A/V^2$ , $\mu_n = 2.2\mu p$ . Determine the beta ratio, $B_n/B_p$ , for a midpoint (switching threshold) of $V_M = 1.3V$ | 3<br>(CO 2) |
| Q7 |   | Design a full adder using MUX. Your answer should contain the full truth table , logical expression & explanation and logic circuit.                                                                                                                | 3<br>(CO 3) |
| Q8 |   | Design and Explain the functioning of an EX-OR gate using Transmission gate Logic.                                                                                                                                                                  | 3<br>(CO 2) |