

JK Lakshmipat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), April- May 2015

B. Tech., B.Tech. +M.Tech and B.Tech+MBA in Computer Science and Engineering, Semester IV

Roll No.....

CSE403: COMPUTER ARCHITECTURE AND ORGANIZATION

Time: 03 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of CALCULATOR is not allowed

Q.1A Objective type multiple choice questions (10 questions @ 1 mark)

10

- i. In a multiprogramming system, which of the following is used
(A) Data parallelism (B) Paging concept
(C) L1 cache (D) None of the above
- ii. Manipulation of individual bits of a word is often referred to as
(A) Bit twiddling (B) Bit swapping
(C) Micro-operation (D) None of these
- iii. Zero address instruction format is used for
(A) RISC architecture.
(B) CISC architecture.
(C) Von-Neumann architecture.
(D) Stack-organized architecture.
- iv. The ASCII code for letter A is
(A) 1100011 (B) 1000001
(C) 1111111 (D) 0010011
- v. Dynamic RAM consumes _____ Power and _____ then the Static RAM.
(A) more, faster (B) more, slower
(C) less, slower (D) less, faster
- vi. Cache memory works on the principle of
(A) Locality of data.
(B) Locality of reference
(C) Locality of memory
(D) Locality of reference & memory
- vii. Which of the memory holds the information when the Power Supply is switched off?
(A) Static RAM (B) Dynamic RAM





	(C) EEROM (D) None of the above	
viii.	In DMA the data transfer is controlled by (A) Microprocessor (B) RAM (C) Memory (D) I/O devices	
ix.	Cycle stealing technique is used in (A) Interrupt based data transfer (B) Polled mode data transfer (C) DMA based data transfer (D) None of these	
x.	The communication between central system and the outside environment is done by A) Input-output subsystem B) Control system C) Memory system D) Logic system	
Q.2	Short answer type questions (4 questions @ 2.5 marks)	10
i.	What is an I/O command?	
ii.	What is the need of control unit in a computer?	
iii.	What is Paging?	
iv.	How the programs are run through virtual memory?	
Q.3A	Evaluate $A*B+F*(B*D+C/E)$ in assembly language using two and three address format?	05
Q.3B	When should the pages in the memory be replaced?	05
Q.4A	Why does DMA have priority over CPU when both when both request a memory transfer?	05
Q.4B	What is daisy chaining priority method of interrupt?	05
Q.5A	State the advantages of cache memory?	05
Q.5B	Differentiate between synchronous and asynchronous bus.	05
OR		
Q.5B	Differentiate between static and dynamic RAM.	05
Q.6A	How will you improve the performance of cache memory?	05

Q.6B	A computer has 65536 MB of memory. Each word in this computer is sixteen bytes. How many bits are needed to address any single word in memory?	05
Q.7A	How many memory chips of (128×8) are needed to provide a memory Capacity of 4096×16 ?	05
Q.7B	What handling techniques are used to handle page faults?	05
	OR	
Q.7B	Which are different mapping techniques used in cache memories and their relative merits and demerits.	05
Q.8A	Determine the number of clock cycles that it takes to process 200 tasks in a 6 segment pipeline? Write down Flynn's classification of computers?	10
Q.8B	What is the difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?	05
	OR	
Q.8B	What is the need of memory management hardware? Explain demand paging and swapping?	05
Q.9A	Which are the techniques for addressing an I/O device?	10
Q.9B	What are different modes of data transfer in an I/O explain interrupt driven data transfer?	05
	OR	
Q.9B	Differentiate synchronous and asynchronous data transfer over a bus in computer organization?	05