

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/ Backlog), November-December 2015

B. Tech in Electronics and Communication / Electrical Engineering, Semester VI

Roll No.....

ECE 726: VHDL

Time: 3 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A Objective type multiple choice questions (10 questions @ 1 mark) 10

- i. The statement "*An entity X, when used in another entity Y, becomes a component for the entity Y*" is (a) wrong (b) partially correct (c) correct (d) none of these.
- ii. An "**inout**" declaration is (a) an input signal (b) an output signal but can be read back by the entity (c) a bidirectional signal (d) none of these
- iii. Which is a valid declaration for the identifiers? (a) `_OR7_` (b) `reg_2` (c) `2__FFT` (d) `reg_#N`
- iv. The operator "`<=`" is (a) a relational operator (b) a logical operator (c) a basic operator (d) none of these.
- v. The resolved logic in VHDL is used to drive a signal by (a) 2 inputs (b) 3 inputs (c) only one input (d) none of these.
- vi. To model a wire connection in VHDL what type of VHDL declaration is used? (a) a variable (b) an operator (c) a signal (d) none of these.
- vii. In the 8254 Timer/Counter the valid counting operations allowed are (a) BCD (b) Binary (c) Both (d) None of these.
- viii. Which mode of 8254 timer device is used generate a mono shot pulse? (a) Mode 1 (b) Mode 5 (c) Mode 4 (d) Mode 3.
- ix. In which type of modeling process keyword is used? (a) Structural (b) Behavioral (c) Dataflow (d) none of these.
- x. For proper synthesis, use of latches is avoided if it is not absolutely necessary. (TRUE/FALSE).

Q.2 Short answer type questions (4 questions @ 2.5 marks) 10

- Q.2A Draw a circuit using D Flip-Flops which divides the clock by four (Divide-by-4).
- Q.2B Compare between a Mealy and Moore Finite State Machine (FSM).
- Q.2C Implement the expression $f(A, B, C) = A'B + AB'$ using a 2:1 multiplexer.
- Q.2D List at least five operations which an ALU can perform.

- Q.3A For the following VHDL Code listed below (a) Draw the Circuit (b) Give the truth table. 05

```
LIBRARY ieee;
USE IEEE.std_logic_1164.ALL;

ENTITY CKT1 IS
    PORT (a,b, c : IN std_logic;
          x : OUT std_logic);
END ENTITY CKT1;

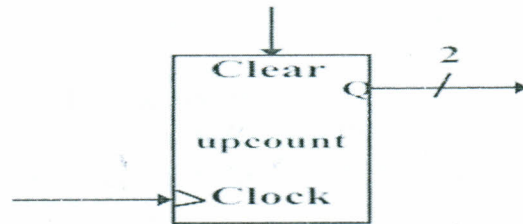
ARCHITECTURE CKT1_arch OF CKT1 IS
    SIGNAL x1, y1: std_logic;
BEGIN
    PROCESS (a, b, c) IS
    BEGIN
        x1<= a XOR b;
        y1 <= x1 NOR c;
        x <= NOT y1;
    END PROCESS;
END;
```

- Q.3B For the truth table given below, find the expression of F. After minimizing the expression for F, write VHDL code to implement the expression. 05

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

- Q.4A What do you understand by an FPGA and an ASIC device? Draw the complete ASIC design flow chart. 05
- Q.4B How many types of instructions will you find on a typical CPU? Discuss the instruction format for a **double-word** instruction in a typical CPU. 05

Q.5A Write the VHDL **behavioral codes** for a 2-bit **asynchronous** counter as shown in the figure.



05

Q.5B Write the VHDL **structural codes** for the circuit described by the following expressions:

05

$$Y = D \text{ XOR } E$$

$$D = A \text{ NAND } B \text{ and}$$

$$E = B \text{ NOR } C$$

Q.6A Perform **Booth's Algorithm** based multiplication for the numbers shown below by showing all the necessary steps for multiplication.

05

$$-7 \times 5$$

Q.6B Using **Restoration Method** perform division for the numbers shown below by showing all the necessary steps.

$$12 \div 7$$

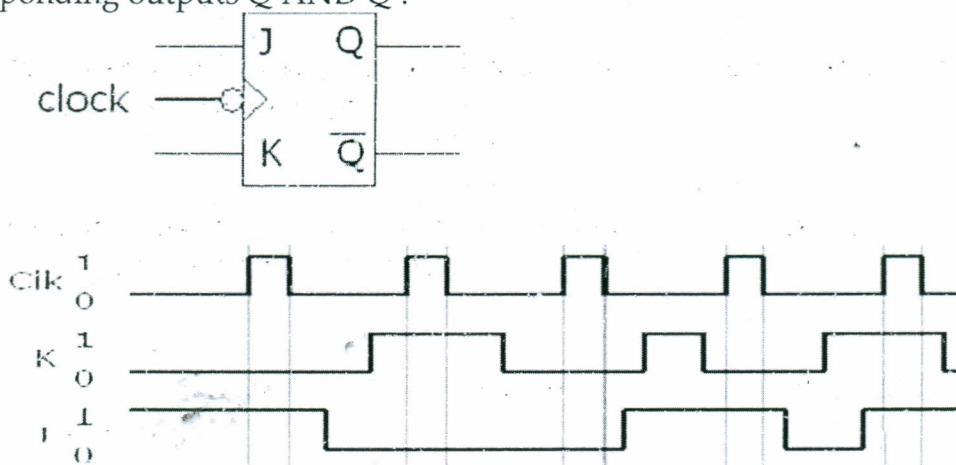
OR

Q.6B Draw the logic diagram of a 2-bit comparator circuit and then cascade two such comparators to get a 3-bit comparator.

05

Q.7A Complete the timing diagram for the circuit shown below i.e. draw the corresponding outputs Q AND Q'.

05



Q.7B Construct a JK flip-flop from a D flip-flop using the method discussed in class.

05

OR

Q.7B What do you understand by Modeling of Digital Systems? Briefly compare the modeling techniques used in VHDL.

05

- Q.8 You need to design a simple Moore Counter which counts in the normal sequence as 0, 1, 2, 3 repeatedly. 10
- (a) Give the state diagram that will realize this sequence.
 - (b) Derive the state table for implementing the circuit using D flip-flops.
 - (c) Use K-maps to compute optimal expressions for the inputs to the D flip-flops.
 - (d) Show the final circuit.

- Q.9A Assume the structure of a Full Adder circuit is already given to you, the component description for which is as below: 10

```
COMPONENT FULL_ADDER
  PORT (X, Y, Bin : IN bit;
        Cout, Sum : OUT bit);
END COMPONENT;
```

- (i) Draw and label a new circuit using the circuit given above which performs the operation $S = A + B$ for 4-bit inputs.
 - (ii) Write the structural VHDL code for the new circuit as in (i), given that the structure of a Full Adder is already available, stated earlier. (**Hint:** Use **port map**, don't define several components, just use the above component)
- Q.9B Implement the following 4-input Boolean function using a single 8:1 multiplexer by considering B as the residue. Draw the circuit also. 10
- $$F = \sum m(0, 1, 4, 7, 8, 10, 14, 15)$$
- OR
- Q.9B Draw the interfacing circuit for an 8254 timer whose port addresses are given as 70h - 73h. Write initialization codes to configure: 10
- (i) Counter 1 in mode 4, MSB only, binary with a count value of 4370_H.
 - (ii) Counter 2 in mode 5, LSB+MSB, BCD with a count value of 97_H.

*****ALL THE BEST*****