



JK Lakshmi Pat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Backlog), May 2026

BTech, Semester II

Roll No.....

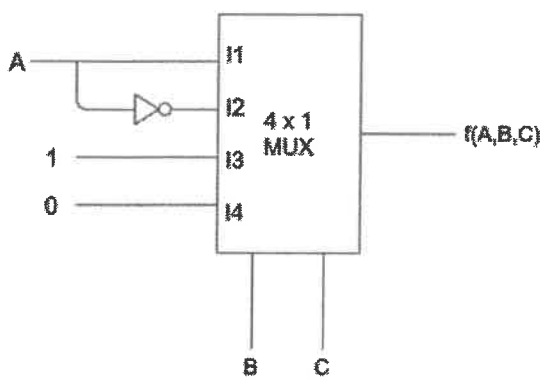
EE1120: Digital Circuit and Systems

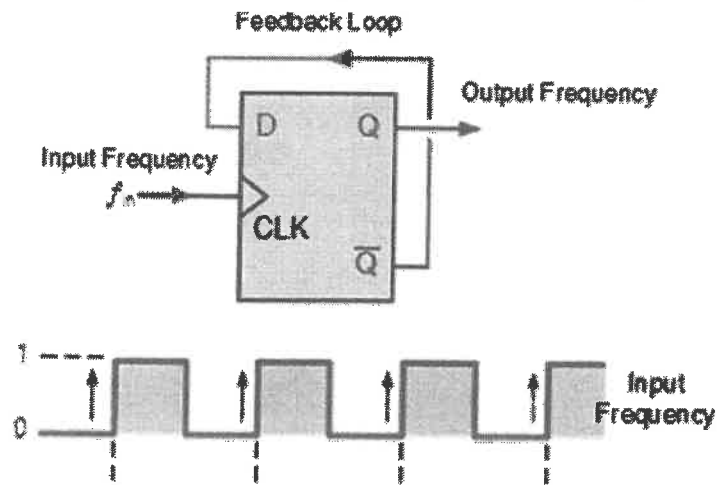
Time: 2.5 hours

Max. Marks: 30

Instructions to students:

1. Do not write anything other than your roll number on the question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

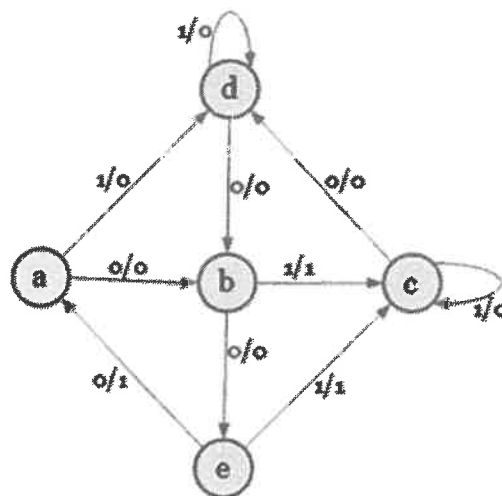
Q.1	Draw the symbol, truth table and expression for all the logic gates. Also draw all the logic gates using NAND gate only.	04 (CO1)
Q.2	Design and explain a full adder circuit using required tables, expressions and diagrams.	03 (CO3)
Q.3	What will be the output expression of the following circuit. Also draw the simplified logic diagram using 2 input gate. 	03 (CO3)
Q.4	Simplify the Boolean function using and draw using AOI gates $F(A, B, C, D) = \Sigma(2,3,4,5,6,7,8,9,10,11,13,14)$	03 (CO3)
Q.5	Discuss the working of JK Flip flop with proper diagram. Also show the truth table, charateriscis table, Characteristic equation, Excitation table and Symbol (both positive and negative edge triggered).	04 (CO4)
Q.6	Discuss in detail (working and output frequency) for the following circuit. Initially the circuit is at rest. Also complete the waveform given below for the output frequency.	04 (CO4)



Q.7 Design a MOD 4 (0 to 3 to 0...) synchronous up Counter (using negative edge triggered T FF). 04 (CO5)

OR

Q.7 Determine the reduced state diagram for the given state diagram. 04 (CO5)



Q.8 Design a Mealy FSM to detect sequence 110. Draw state diagram and state table for the overlapping case. Show the output for the following sequence. 05 (CO5)

110110111010110