

JK Lakshmipat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination, December 2022

B. Tech. in Electrical and Electronic Engineering, Semester V

Roll No.....

Course Code: EE1102 Analog Circuits

Time: 2:30 hours

Max. Marks: 30

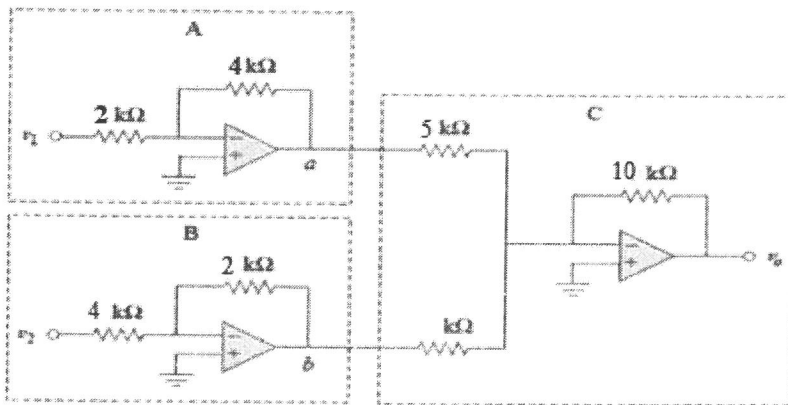
Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Answer all questions

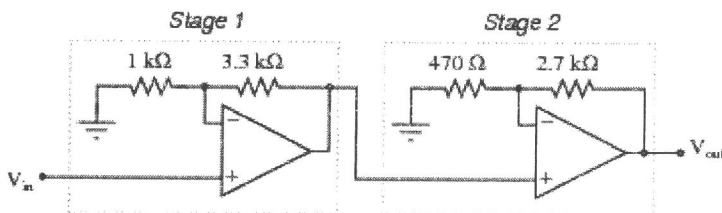
- (1) For $V_1 = 2\text{ V}$ and $V_2 = 4\text{ V}$, find V_0 in the circuit below.

[4]
(LO1 & LO2)



- (2) Calculate the voltage gain for each stage of this amplifier circuit then calculate the overall voltage gain:

[4]
(LO1 & LO2)



- (3) Design a second order low pass filter with at a cut off frequency of 5 kHz with a pass band gain of 4.

[4]
(LO5 & LO7)

- (4) Develop a 4-bit R-2R ladder network converter and determine:

[4]
(LO6)

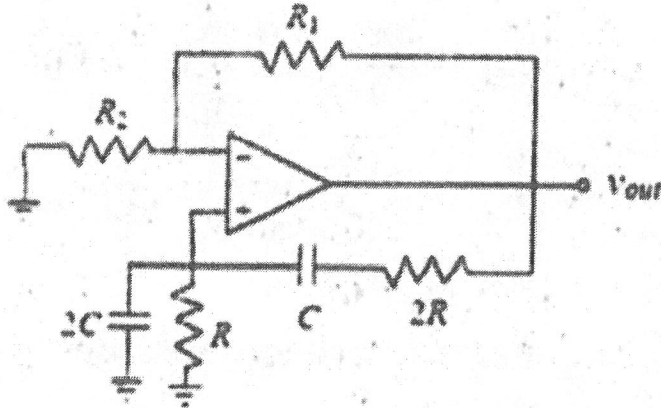
- (i) Resolution of converter for reference voltage 5 V.
- (ii) Output voltage when inputs b_0, b_1, b_2 and b_3 are at 2 V.
- (iii) Output voltage when inputs $b_0 = b_1 = b_2 = 5\text{ V}$ and $b_3 = 0$.

- (5) Design a Hartley oscillator to produce a sine wave of frequency 1 GHz and fraction of feedback is 3 and uses a capacitance of $C_1 = 0.01\text{ }\mu\text{F}$.

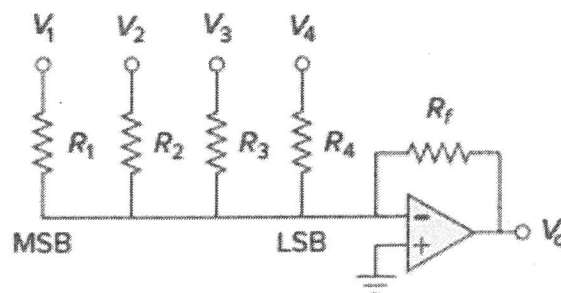
[4]
(LO5 & LO6)

- (6) From the circuit shown in the below figure has an ideal op-amp, determine

[4]
(LO5 & LO6)



- (a) Type of oscillator
(b) Frequency of oscillation
(c) Relation between R_1 and R_2
(d) Feedback gain factor
- (7) Develop a voltage amplifier has input resistance of $10\text{ k}\Omega$ and output impedance of $100\text{ k}\Omega$. It is used in negative feedback circuit with 20% feedback and open loop gain is 200. For a closed loop amplifier, calculate
- (a) Closed loop input impedance
(b) Output impedance
(c) Lower cut-off frequency
(d) Upper cut-off frequency
(e) Bandwidth
- (8) In the DAC circuit below, $R_f = 10\text{ k}\Omega$, $R_1 = 10\text{ k}\Omega$, $R_2 = 20\text{ k}\Omega$, $R_3 = 40\text{ k}\Omega$, and $R_4 = 80\text{ k}\Omega$. [2] (LO4)



Obtain the output voltage for the inputs:

- (a) 0 0 0 0 (b) 0 0 0 1 (c) 0 0 1 0 (d) 1 1 1 1

Consider $V_{\text{ref}} = 1\text{ V}$.