

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Theory Examination, May 2026

B. Tech. VI, Semester

Roll No.....

EE1231 : Digital Verification and Testing

Time: 2 hours

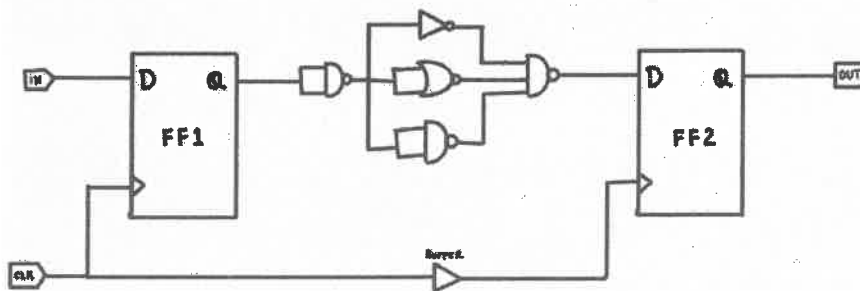
Max. Marks: 30

Instructions to students:

1. Do not write anything other than your roll number on the question paper.
2. Use of calculator is allowed.
3. **There are total 6 questions**

Q.1 a) Consider the following circuit.?

3 Marks
[CO3]



Delay values of Flipflop and Combinational circuit are: $t_{\text{setup}} = 3\text{ns}$ and $t_{\text{hold}} = 2\text{ns}$. The delay of the buffer is $t_{\text{buf}} = 2\text{ns}$.

Delay	$t_{\text{clk-q}}$	t_{NAND3}	t_{NOT}	t_{NOR}	t_{NAND2}
Max	3 ns	2.5 ns	1 ns	2.5 ns	2 ns
Min	2 ns	1.5 ns	0.3 ns	1.5ns	1.2 ns

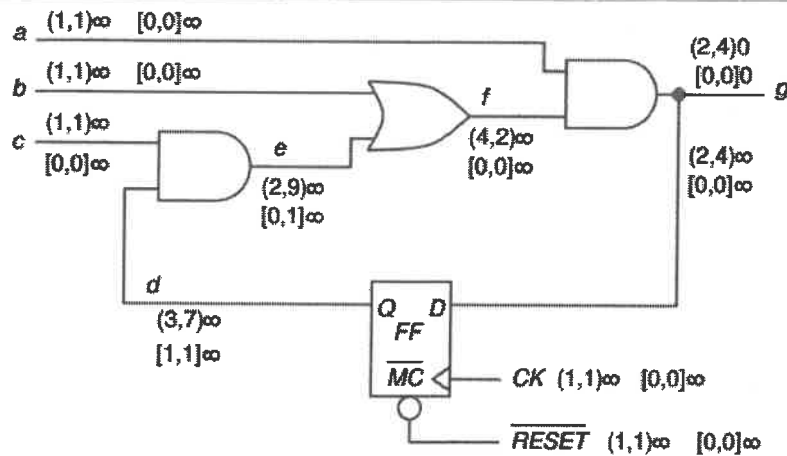
Calculate the maximum frequency at which the given circuit can operate without failure

b) Design the correct hold constraint equation for the circuit given in question 1. a

2 Marks
[CO3]

Q.2 For the given circuit Compute the combinational SCOAP testability measures (both controllability and observability).

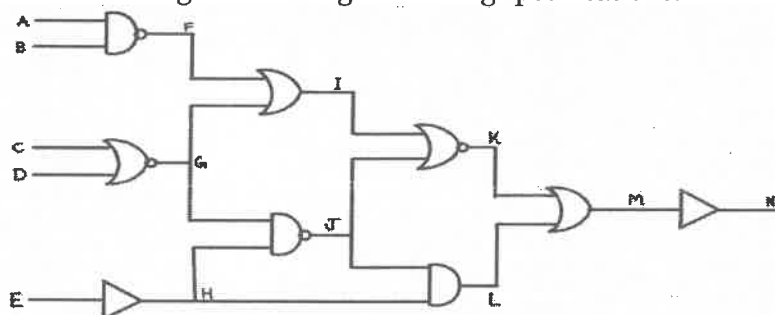
5 Marks
[CO2]



3. Develop a testing technique for efficient debugging of digital circuits by using IEEE 1149.1 (JTAG) standard in test interfaces. 3 Marks
[CO1]

4. Draw and explain the verification environment in UVM. 4 Marks
[CO1]

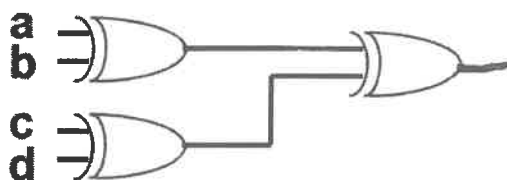
5. Consider the following circuit and given timing specifications. 6 Marks
[CO4]



Logic gate	Rise delay(ns)	Fall delay(ns)
NAND	4	3
NOR	3	5
AND	2	3
OR	5	4
Buffer	1	2

Find RAT, AT, and SLACK of each node and trace the critical/worst path for the given circuit?

6. Create a Reduced Binary Decision Diagram for the following circuit: 4
[CO3]



7. Design and explain each design step of a 1 clock fifo register with labeled diagram the working of 3
[CO4]