

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), January 2022
BCA, Semester I

Roll No.....

CS1117: Computer Organisation and Systems

Time: 3 hours

Max. Marks: 60

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

Q.1A Do the following for signed number representation. 04

- i. +8 - 19
- ii. - 8 - 19

Q.1B Consider a pipeline having 5 phases with duration 40, 60, 50, 90 and 80 ns. Given latch delay is 20 ns. Calculate- 06

- i. Pipeline cycle time
- ii. Non-pipeline execution time
- iii. Speed up ratio
- iv. Pipeline time for 2000 tasks
- v. Sequential time for 2000 tasks
- vi. Throughput

Q.2 Write and explain an 8086 assembly program to add two 16-bit numbers, 20F0 (Hexadecimal) and F0F0 (Hexadecimal). Store the result at 3004 and 3006 memory address. 10

Q.3A Explain the concept of locality of reference in cache memory. 04

Q.3B The memory access time is 2 ns for a read operation with a hit in cache, 7 ns for a read operation with a miss in cache, 3 ns for a write operation with a hit in cache and 12 ns for a write operation with a miss in cache. Execution of a sequence of instructions involves 150 instruction fetch operations, 90 memory 06

operand read operations and 60 memory operand write operations. The cache hit ratio is 0.8. Calculate

- i. Total time required for read operations.
- ii. Total time required for write operations.
- iii. Calculate the average memory access time (in ns) in executing the sequence of instruction?

Q.4A Explain the concept of Virtual Memory using suitable diagram. 04

Q.4B Explain the concept of memory interleaving. Implement it using higher order interleaving method. 06

Q.5 A computer has memory unit of $64\text{ K} \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. 10

- i. What is the size of address and data bus?
- ii. How many bits are there in the tag, index, block and word fields of the address formula?
- iii. How many blocks can be accommodate in cache?

Q.6A Explain the use of PCI and SCSI interface in Computer. 04

Q.6B Consider a disk drive with the following specification: 06

16 surfaces, 256 tracks/surface, 256 sectors/track, 1KB/sector, rotation speed 1800 rpm. The disk is operated in cycle stealing mode where, whenever one-byte word is ready it is sent to memory, similarly for writing the disk interface reads a 4-byte word from the memory in each DMA cycle. Memory cycle time is 30 ns. Calculate the maximum percentage of time that the CPU gets block.