

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/Backlog), Nov. 2016

B. Tech. in Electronics & Communication Engineering, Semester III

Roll No.....

ECE306: DIGITAL ELECTRONICS

Time: 3.0 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Non-Programmable calculator is allowed.

Q.1A Objective type multiple choice questions (10 questions @ 1 mark)

10

i. Consider the given circuit

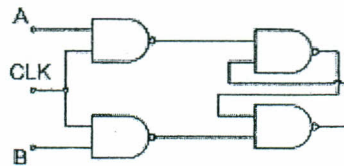


Fig.1

In this circuit, the race around

(A) does not occur

(B) occurs when CLK = 0

(C) occurs when CLK = 1 and A = B = 1

(D) occurs when CLK = 1 and A = B = 0

ii. A 64-bit word consists of _____ bytes.

iii. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is.....

iv. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles.....

v. For designing 128 x 16 ROM, the size of decoder is

vi. What are the different types of RAM?

vii. What do you understand with ASCII code?

viii. What do you understand with PAL?

ix. Write the IC number of two inputs EXOR gate.

x. Draw the symbol for negative edge triggered JK Flip flop.

xi. How many bits in 4 Giga Bytes?

xii. The PAL has an AND and OR structure similar to a PROM, but in the PAL the inputs to the AND gates are programmable, whereas the inputs to the OR gate are hard-wired.(True/False)

Q.2 Each Question is of 2.5 marks

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- Explain the need and advantages of using programmable logic devices in digital system design.
- Draw the state transition diagram for the logic circuit shown below

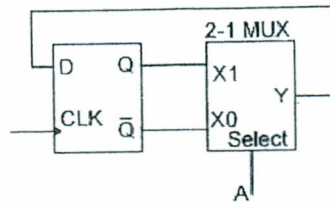


Fig. 2.1

- Give the latch diagram of Dynamic RAM?
- What will be value for P, Q and R for output $y = 1$?

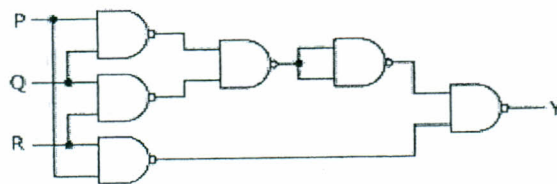


Fig.2.2

Q.3A A safe has 5 locks v, w, x, y and z; all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner.

05

- Mr. P has keys for locks v and x.
- Mr. Q has keys for locks v and y.
- Mr. R has keys for locks w and y.
- Mr. S has keys for locks x and z.
- Mr. T has keys for locks v and z.

Find the minimum number of executives required to open the safe. Also implement it using NAND gates Only.

Q.3B The logic function implemented by the circuit below is (ground implies logic 0)

05

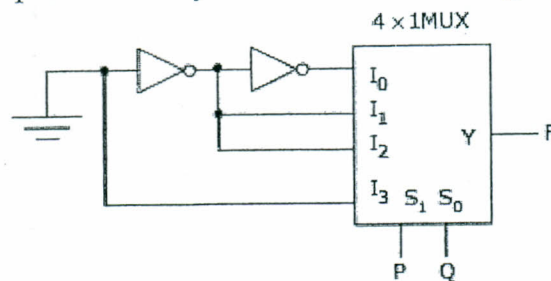


Fig.3

- What will be the 8 bit 1's complement representation of decimal number (-75).
- Multiply $(888)_{10}$ with $(EFA)_{16}$.

05

Q.4B Match the logic gates in Column A with their equivalents in Column B.

05

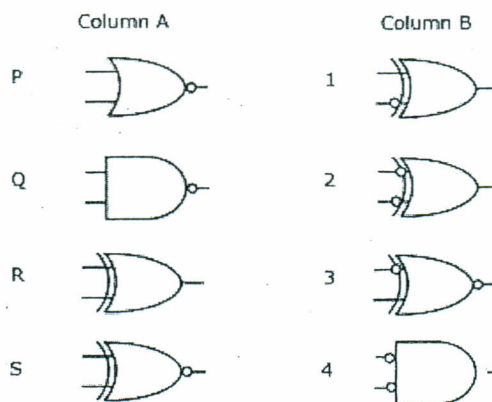


Fig. 4

Q.5A Explain the ASM block using State box, Decision box and Conditional box.

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Q.5B Consider the following two codes and answer the given questions.

05

Code A	Code B
000101	0001
001011	0011
010011	0110
100010	0111

- $d_{\min}$ for code A and code B.
- Detects single error
- Detects double error
- Corrects single errors
- Corrects double errors

Q.6A We can expand the word size of a RAM by combining two or more RAM chips. 05
For instance, we can use two 32×8 memory chips where the number 32 represents the number of words and 8 represents the number of bits per word. To obtain a 32×16 RAM, the number of words remains the same but the length of each word will two bytes long. Draw a block diagram to show how We can use two 16×4 memory chips to obtain a 16×8 RAM.

Q.6B Derive the equations for a to d outputs for a BCD to seven segment display board. 05

OR

Q.6B Assuming that flip-flops are in reset condition initially, the count sequence 05
observed at Q_A for the four clock pulses in the circuit shown is

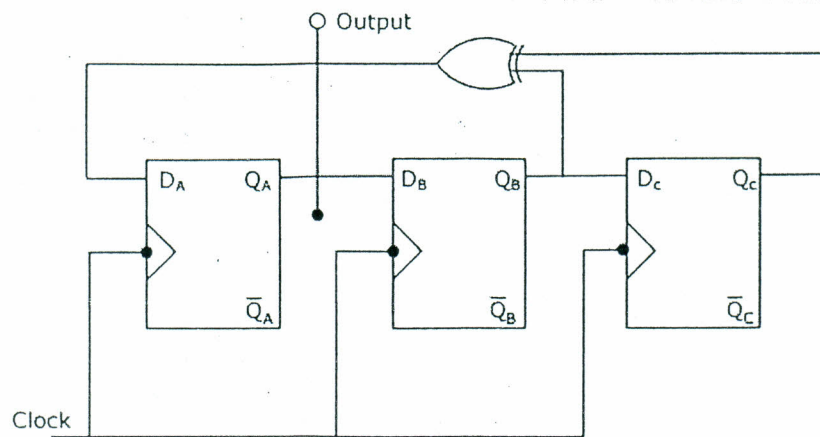


Fig. 5

Q.7A The outputs of the two flip-flops Q1, Q2 in the figure shown are initialized to 0,0. The sequence generated at Q1 upon application of 4th clock signal is 05

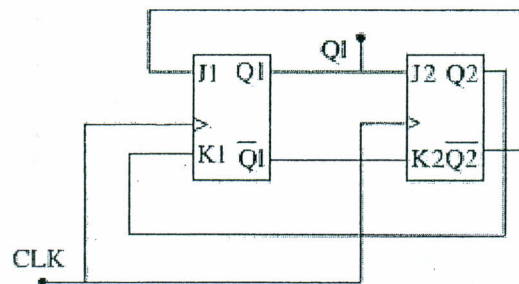


Fig.6

Q.7B Implement the following equations using a suitable PAL circuit. 05

$$A(x,y,z,w) = \sum m(3,5,6,7,8,11,13,14,15)$$

$$B(x,y,z,w) = \sum m(0,1,5,6,8,9,11,13,14)$$

Q.8 A sequential circuit has two flip flops (A and B), two input x and y, and one output z. The flip-flop input equations and circuit output equation are 10

$$J_A = B'x + By'$$

$$K_A = B'xy'$$

$$J_B = A'x$$

$$K_B = B + xy'$$

$$z = Bxy + Ax'y'$$

- Draw the logic diagram the circuit.
- Tabulate the state table.
- Derive the state equation for A and B.

OR

Q.8 Design a Mod 9 ripple counter using T flip flop and draw the output waveforms. 10

Q.9A Draw the reduced state diagram for the following state diagram. 07

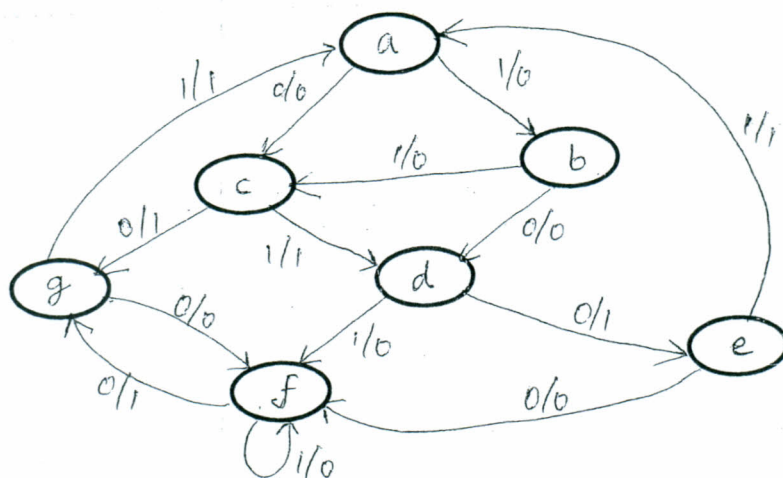


Fig.7

OR

- Q.9A Implement the following equations using a suitable PLA circuit.
- $$A(x,y,z,w) = \sum m(3,7,8,9,11,15)$$
- $$B(x,y,z,w) = \sum m(3,4,5,7,10,14,15)$$
- $$C(x,y,z,w) = \sum m(1,5,7,11,15)$$

07

- Q.9B Explain even and odd parity 4 bit BCD codes.

03

- Q.10 Implement the following state diagram using JK flip flop.

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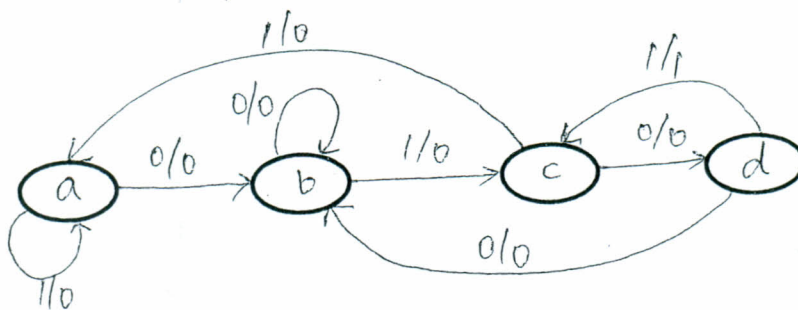


Fig. 8