

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), May 2019

B. Tech. in Computer Science and Engineering, Semester IV

Roll No.....

CSE403: COMPUTER ARCHITECTURE AND
ORGANIZATION

Time: 02 hours

Max. Marks: 50

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A Demand paging system with 4 page frames for page replacement. Give a diagram of all pages in memory after each page fault, for the following reference string: 05

2, 4, 5, 4, 5, 9, 2, 7, 4, 8, 9, 1, 6, 2, 2, 5, 3, 8, 7, 9, 2, 3

Show the content of memory, and indicate whenever there is a page fault if

- I). Optimal Replacement algorithm is used.
- II). LRU algorithm is used.
- III). FIFO algorithm is used.

Q.1B How has RISC design philosophy impacted these technology trends, as well as processor performance? are there any implications of Amdahl's Law for processor performance optimization? 05

Q.2A Consider a disk with a sector size of 512 bytes, 2000 tracks per surface, 50 sectors per track, five double-sided platters, and average seek time of 10 msec. 05

1. What is the capacity of a track in bytes? What is the capacity of each surface?

What is the capacity of the disk?

2. How many cylinders does the disk have?

3. Give examples of valid block sizes. Is 256 bytes a valid block size? 2048? 51200?

4. If the disk platters rotate at 5400 rpm (revolutions per minute), what is the maximum rotational delay?

5. If one track of data can be transferred per revolution, what is the transfer rate?

Q.2B Which RAID configuration should Raj use if he wants to optimize the database system for workloads consisting of small random reads and writes and why? which is better for fault tolerance? 05

Q.3A	Consider the following code sequence having five instructions from I1 to I5.- Instructions I1 : ADD R1, R2, R3 I2: MUL R7, R1, R3 I3: SUB R4, R1, R5 I4: ADD R3, R2, R4 I5: MUL R7, R8, R9 I). Identify the True dependencies, anti-dependencies and output dependencies of the above instruction? II). Remove dependencies by providing stalls? II). Difference between dependency and hazard?	10
Q.3B	Which is usually faster – an asynchronous or a synchronous bus? Why would you ever use the slower type?	05
Q.4	Suppose we had a block transfer from an I/O device to memory. The block consists of 1024 words and one word can be transferred at a time. In how many ways we can transfer block? Also indicate the number of interrupts needed to transfer a block? Why we cannot connect the I/O devices directly to the processor bus?	05
Q.5A	Consider you have 4096 x 16 RAM chips to build a main memory bank. A. How many of these chips are needed to provide a memory capacity of 6 GB? B. How many lines of the address bus must be used to access 6GB of memory (one byte at a time)? How many of these lines will be common to all the chips? C. How many lines must be decoded in order to select the right chip (activate chip select)?	05
Q.5B	How does instruction set, compiler technology, CPU implementation and control and cache and memory hierarchy affect the CPU performance and justify the effects in terms of program length, clock rate and effective CPI	05