

[JK LAKSHMIPAT UNIVERSITY, JAIPUR
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EndTerm Examination (Regular/Backlog), November 2016
B. Tech/ M. Tech (as applicable) in ECE, CSE and EE, Semester III

Roll No.....

ECE 301: Electronic Devices and Circuits

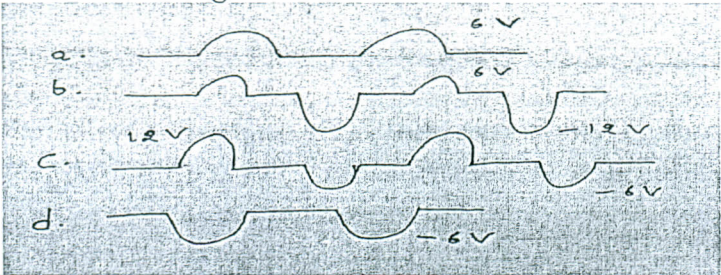
Time: 3 hours

Max. Marks: 100

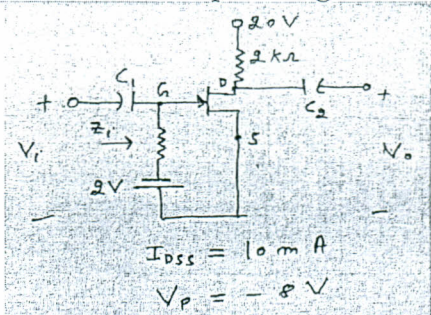
Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

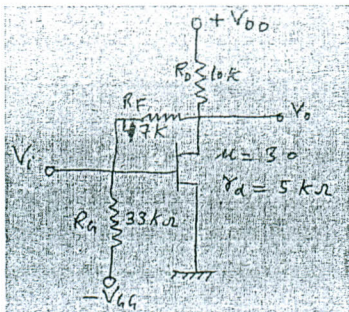
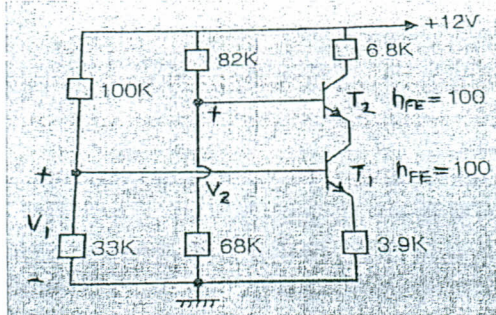
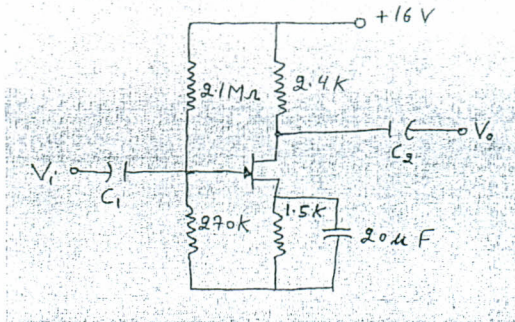
Q.1A	Objective type multiple choice questions (10 questions @ 1 mark)	10
i.	In an intrinsic semiconductor the free electron concentration depends on a. Effective mass of electron only. b. Effective mass of holes only. c. Temperature of the semiconductor. d. Width of the forbidden energy band of the semiconductor.	
ii.	A semiconductor is irradiated with light such that carriers are uniformly generated throughout its volume. The semiconductor is N-type with $N_D = 10^{19}/\text{cm}^3$. If excess electron concentration in the steady state is $\Delta n = 10^5/\text{cm}^3$ and $\tau_p = 10 \mu\text{sec}$. (minority carrier life time) the generation rate due to irradiation a. Is 10^{20} e-h pairs/cm^3/S b. Is 10^{24} e-h pairs/cm^3/S c. Is 10^{10} e-h pairs/cm^3/S d. Cannot be determined, the given data is insufficient.	
iii.	The resistivity of a uniformly doped n-type silicon sample is $0.5 \Omega\text{-cm}$. If the electron mobility (μ_n) is $1250 \text{cm}^2/\text{V-sec}$ and the charge of an electron is 1.6×10^{-19} Coulomb, the donor impurity concentration (N_D) in the sample is a. $2 \times 10^{16}/\text{cm}^3$ b. $1 \times 10^{16}/\text{cm}^3$ c. $2.5 \times 10^{16}/\text{cm}^3$ d. $2 \times 10^{15}/\text{cm}^3$	
iv.	The threshold voltage of an N-channel MOSFET can be increased by a. Increasing the channel dopant concentration b. Reducing the channel dopant concentration c. Reducing the GATE oxide thickness d. Reducing the channel length.	
v.	MOSFET can be used as a. Current controlled capacitor b. Voltage controlled capacitor c. Current controlled inductor d. Voltage controlled inductor	
vi.	An N-channel JFET has a pinch-off voltage $V_p = -5\text{V}$, $V_{DS(\text{max})} = 20\text{V}$ and $g_m = 2 \text{mA}/\text{V}$. The min 'ON' resistance is achieved in the JFET for	

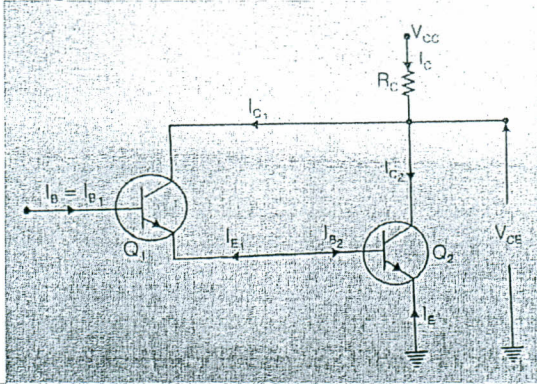
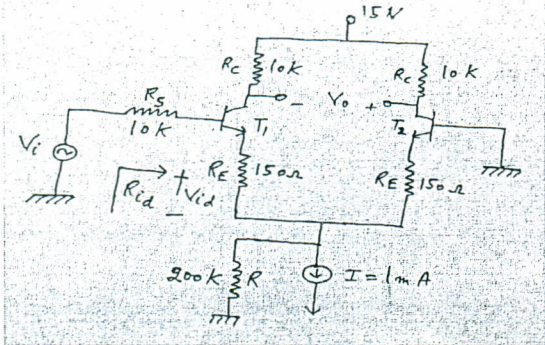
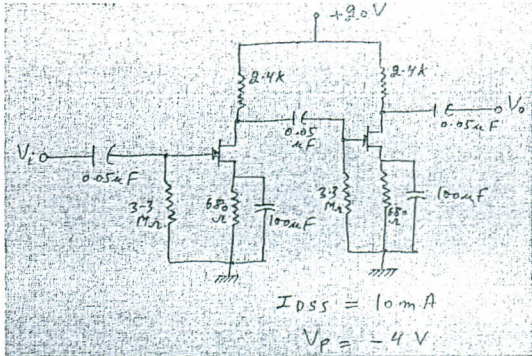
	a. $V_{GS} = -7V$ and $V_{DS} = 0V$ b. $V_{GS} = 0V$ and $V_{DS} = 0V$ c. $V_{GS} = 0V$ and $V_{DS} = 20V$ d. $V_{GS} = -7V$ and $V_{DS} = 20V$	
vii	For the circuit shown below, assume that the Zener diode is ideal with a breakdown voltage of 6 volts. The waveform observed across R is 	
viii	Each transistor in the Darlington pair (see fig. below) has $h_{fe} = 100$. The overall h_{fe} of the composite transistor neglecting the leakage currents is a. 10000 b. 10001 c. 10100 d. 10200	
ix	An n-channel JFET has $I_{DSS} = 1mA$ and $V_p = -5V$. Its maximum transconductance is _____.	
x	A cascode Amplifier stage is equivalent to a. A common emitter stage followed by a common base stage b. A common base stage followed by an Emitter follower c. An Emitter follower followed by a common base stage d. A common base stage followed by a common emitter stage	

Q.2	Short answer type questions (4 questions @ 2.5 marks)	10
i	Explain why NMOS is preferred over PMOS by IC fabrication?	
ii	Explain Short channel length effect in FET?	
iii	Explain Base modulation (or base narrowing) in Bipolar junction transistor?	
iv	Describe how an FET can be used as a voltage variable resistor (VVR)?	

Q.3A	Draw and explain the characteristics of an N-MOSFET. Calculate the minimum value of V_{DS} required for an NMOSFET to operate in pinchoff condition when $V_{GS} = 1V$, $V_p = -2V$, $I_{DSS} = 10mA$. Also find the corresponding drain current.	05
Q.3B	For the circuit shown below. Calculate a. g_m b. r_d c. Z_i d. Z_o e. A_v 	05

Q.4A	Explain Hall effect in materials and how the phenomenon of Hall effect can be used to determine whether a semiconductor is n-type or p-type?	05
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4B	Define Hall coefficient R_H . Obtain an expression for R_H in terms of Hall voltage V_H .	05
Q.5A	Draw the low frequency small signal models of FET (common source configuration) and BJT (common emitter configuration), and compare the two models.	05
Q.5B	Determine the voltage gain $A_v = V_o/V_i$ for the amplifier circuit shown below. V_i is the input voltage between the gate terminal and ground. Neglect all capacitances.	05
		
Q.6A	For the circuit shown in figure (A), calculate the Q point for both transistors. Assume silicon transistors, $V_{BE} = 0.7$ V.	05
		
Q.6B	Write down the expression for Fermi-Dirac distribution function. Show that the probability that a state ΔE above the Fermi level, E_F is filled equals the probability that a state below E_F by the same amount ΔE is empty.	05
	OR	
Q.6B	An abrupt Si P-N junction has $N_A = 10^{23}/\text{m}^3$ on P-side and $N_D = 10^{21}/\text{m}^3$ on N-side. Calculate the value of the contact potential and the total width of the depletion region under unbiased condition at 300K. The intrinsic carrier concentration of Si is $1.5 \times 10^{16}/\text{m}^3$ and relative permittivity is 11.8.	05
Q.7A	Determine I_{DQ} and V_{GSQ} , V_D , V_S , V_{DS} and V_{DG} for the network shown below.	05
		

Q.7B	For the circuit in the fig. (A) $\alpha_1 = 0.98$, $\alpha_2 = 0.98$, $V_{CC} = 24$, $R_C = 120 \Omega$ and $I_E = -100\text{mA}$. Calculate the current I_{C1} , I_{B1} , I_{E1} , I_{B2} , I_{C2} and I_C , the voltage V_{CE} and the ratios I_C/I_B and I_C/I_E . Neglect reverse saturation currents	05
		
OR		
Q.7B	Explain the effect of internal capacitance on bandwidth in common emitter configuration. (Hint: use Miller's theorem)	05
Q.8A	Derive expressions for Z_i , Z_o and voltage gain for self-bias JFET configuration when R_s is unbypassed.	10
Q.9A	Considered the circuit shown in figure (A). the transistors have $\beta = 100$. Determine input differential resistance R_{id} , overall voltage gain V_o/V_i and the worst case common mode rejection ratio if two collector resistance are accurate within $\pm 1\%$.	10
Q.9B	Calculate the dc bias (Q point), voltage gain, input impedance, output impedance and the resulting output voltage for the cascade amplifier shown in figure (B). calculate the load voltage if a $10 \text{ K}\Omega$ load is connected across the output.	10
 Figure A  Figure B		
OR		
Q.9B	Draw Hybrid π model for a bipolar junction transistor in common emitter configuration and derive formulae for the parameters involved in the model.	10

Good Luck