

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination, November 2018

B. Tech. in Electronics & Communication Engineering, Semester III

Roll No.....

ECE310: DIGITAL ELECTRONICS

Time: 3.0 hours

Max. Marks: 80

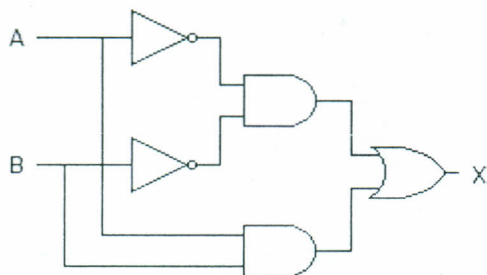
Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Non-Programmable calculator is allowed.

Q.1A Objective type multiple choice questions (10 questions @ 1 mark)

10

- i. Let A and B is the input of a subtractor then the output will be
 - a) A XOR B
 - b) A AND B
 - c) A OR B
 - d) A EXNOR B
- ii. Which of the following logic expressions represents the logic diagram shown?



- a) $X = AB' + A'B$
 - b) $X = (AB)' + AB$
 - c) $X = (AB)' + A'B'$
 - d) $X = A'B' + AB$
- iii. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay ($t_p(\text{total})$) is
 - a) 12 ms
 - b) 24 ns
 - c) 48 ns
 - d) 60 ns
 - iv. In DOWN-counter, each flip-flop is triggered by
 - a) The output of the next flip-flop
 - b) The normal output of the preceding flip-flop
 - c) The clock pulse of the previous flip-flop
 - d) The inverted output of the preceding flip-flop

- v. For realisation of SR flip-flop from JK flip-flop, if $S=1$, $R=0$ & present state is 0 then the excitation input will be
- $J=1$, $K=1$
 - $J=X$, $K=1$
 - $J=1$, $K=X$
 - $J=0$, $K=0$
- vi. A combinational circuit is one in which the output depends on the
- Input combination at the time
 - Input combination and the previous output
 - Input combination at that time and the previous input combination
 - Present output and the previous output
- vii. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
- 2
 - m
 - n
 - None of the Mentioned
- viii. How many bits in a word in 8085 and 8086 microprocessor?
- ix. What do you understand with Microprocessor?
- x. Explain parity method for error detection.

Q.2 Each Question is of 2.5 marks

10

- I. What will the pulse train at the output of the XNOR gate shown in given Fig.?



- Design a 3 bit ring counter using D flip flops.
- What are the different general purpose and special purpose registers in 8085 Microprocessor.
- Find the 9's and 10's complements of the following decimal numbers 12345678

Q.3A Consider the following two codes and answer the given questions.

05

Code A	Code B	Code C
000101	0001	0001001
001011	0011	0011111
010011	0110	0110010
100010	0111	0111110

- $d_{\min}$ for code A, Code B and code C.
- Detects single error.
- Detects double error.
- Corrects double error.

V. Capability of Code C.

Q.3B Design a Full Adder using 3-to-8- line decoder. 05

Q.4A Implement the following expression using a single 8:1 Multiplexer. 05

$$Y(A,B,C,D) = \sum m(0,1,2,6,7,9,10,14)$$

Q.4B Analyze the number of states reduction in the following state table, and tabulate the reduced state table. 05

Present state	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
a	f	B	0	0
b	d	C	0	0
c	f	E	0	0
d	g	A	1	0
e	d	C	0	0
f	f	B	1	1
g	g	H	0	1
h	g	A	1	0

*States are case - insensitive

Q.5A Explain different bits of Flag Register of 8085 using suitable example. 05

Q.5B Implement the following two Boolean functions with a PLA: 05

$$F1(A, B, C) = \sum m(0, 1, 2, 4)$$

$$F2(A, B, C) = \sum m(0, 5, 6, 7)$$

Q.6A Explain the following instruction of 8085 using an example. 03

MOV, LDA

Q.6B What is the race around condition in JK Flip Flop? What are the different methods to overcome this problem? Explain Master-Slave method in detail. 07

OR

Q.6B Design an Asynchronous Counter using JK Flip Flops that counts from 0 to 13 sequence. 07

Q.7A List at least 5 difference between 8085 and 8086 Microprocessor. 03

Q.7B Explain the Architecture of Intel 8085 Microprocessor in detail using suitable diagram. 07

Q.8 A sequential circuit has two JK flip flops A and B, two input x and y, and one output z. The flip-flop input equations and circuit output equation are 10

$$J_A = Bx + B'y'$$

$$K_A = B'xy'$$

$$J_B = A'x$$

$$K_B = A + xy'$$

$$z = Ax'y' + Bx'y'$$

I. Draw the logic diagram the circuit.

II. Tabulate the state table.

III. Derive the state equation for A and B.

OR

Q.8 Deign a BCD to 7 segment decoder (for b,c,d,e,f outputs only). Implement all outputs using logic Gates. 10