

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Special), January 2016

B. Tech in Electronics & Communication Engineering, Semester VII

Roll No.....

ECE728: VLSI DESIGN

Time: 3 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
 2. Assume suitable data wherever required and mention it clearly.
 3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
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Q.1 Objective type multiple choice questions (10 questions @ 1 mark)

10

- i. CMOS logic is probably the best all-around circuitry because of its:
 - a) low power consumption
 - b) packing density
 - c) very high noise immunity
 - d) low power consumption and very high noise immunity
- ii. The time needed for an output to change as the result of an input change is known as:
 - a) noise immunity
 - b) fanout
 - c) propagation delay
 - d) rise time
- iii. Input impedance of MOSFET is
 - a) less than of FET but more than BJT.
 - b) more than that of FET and BJT.
 - c) more than that of FET but less than BJT.
 - d) less than that of FET and BJT.
- iv. In modern the MOSFET, the material used for the gate is
 - a) high - purity silicon
 - b) high - purity silica
 - c) heavily doped poly crystalline silicon
 - d) epitaxially grown silicon
- v. Which of the following boolean expression can not be realized by using four (2 nMOS and 2 PMOS) transistors used in the implementation of a CMOS NAND gate?
 - a) $\bar{A}\bar{B}$
 - b) AB
 - c) A
 - d) $\bar{A}$
- vi. Latch up in CMOS device can be avoided by
 - a) Increasing temp
 - b) doping Control
 - c) Increasing the substrate resistance
 - d) Decreasing substrate doping leve
- vii. Channel current is reduces on application of a more positive voltage to the GATE of the depletion mode n-channel MOSFET (true/false)
- viii. Which of these is an valid identifier:

- a) _c1
 - b) c_10
 - c) process
 - d) 1d
- ix. What is the symbol used for signal assignment?
- a) ==
 - b) :=
 - c) =
 - d) <=
- x. What is the need of Scaling?

Q.2 Short answer type questions (attempt Any FOUR questions @ 2.5 marks)

10

- a) Why does bird's beak region formed?
- b) Why is the size of PMOS transistor chosen to be 2.5 times of an NMOS transistor in CMOS Inverter?
- c) What is channel length modulation?
- d) Find the midpoint voltage, V_X , and output voltage, V_O , for the chain of two nFET pass transistors shown below for the $V_i = 0V$. Assume $V_{DD} = 2.5V$ and $V_{th} = 0.5V$.

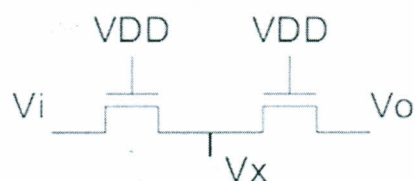


Fig. 1

- e) Why do we require device isolation between MOS transistors that comprise an IC?

- Q.3A Design a CMOS logic gate for the two input XOR function. 05
- Q.3B Explain energy band diagram of MOS structure at surface inversion and derive the equation of threshold voltage. 05
- Q.4A Explain Channel Length Modulation. 05
- Q.4B Explain the basic principle of Pass transistor circuits. Also Explain logic '1' transfer. 05
- Q.5A Explain the LOCOS technique for device isolation. Why it is preferred over the Etched field oxidation technique? 05
- Q.5B Discuss the four components of threshold voltage (V_T) in detail. 05
- Q.6A Write short note (Any ONE) 05
 - a) Comparison of Full-scaling and Constant voltage scaling.
 - b) Power dissipation in Inverters
 - c) MOSFET capacitances
- Q.6B Calculate the threshold voltage V_{T0} at $V_{SB} = 0$, for a polysilicon gate nMOS transistor, with the following parameters: 05

Substrate doping density $N_A = 3.5 \times 10^{16} \text{ cm}^{-3}$
 Polysilicon gate doping density $N_D = 4 \times 10^{20} \text{ cm}^{-3}$
 Gate oxide thickness $t_{ox} = 800 \text{ \AA}$
 Oxide-interface fixed charge density $N_{ox} = 6.5 \times 10^{10} \text{ cm}^{-2}$.

Physical and material constants :

Thermal voltage $kT/q = 26 \text{ mV}$
 Energy Gap of silicon(Si) $E_g = 1.12 \text{ eV}$
 Intrinsic Carrier Concentration of (Si) $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$
 Dielectric constant of vacuum $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$
 Dielectric constant of silicon $\epsilon_{si} = 11.7 \times \epsilon_0 \text{ F/cm}$
 Dielectric constant of silicon dioxide $\epsilon_{ox} = 3.97 \times \epsilon_0 \text{ F/cm}$

OR

Q.6B Implement the following Boolean function using CMOS.

$$F = \overline{(ABC + DE)}$$

Find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assume that $(W/L)_p = 20$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors.

Q.7 Derive the expression for drain current as a function of V_{GS} , V_{DS} and V_{SB} for all three region of operation of MOSFET using Gradual Channel Approximation. 10

OR

Q.7 Explain the functioning of resistive load nMOS inverter and derive critical voltage points V_{OH} , V_{OL} , V_{IL} and V_{IH} .

Q.8 Draw the CMOS Inverter circuit and VTC for different operation regions of the nMOS and pMOS transistor. Derive critical voltage points V_{OH} , V_{OL} , V_{IL} and V_{IH} . 10

OR

Q.8 Explain constant field scaling device reduction strategy and show that the power density does not change in a device scaled using this technique.

Q.9A Explain the fabrication steps of nMOS transistor with necessary figures. 10

Q.9B Explain static, dynamic and short circuit power dissipation in inverters? 10

OR

Q.9B Draw and explain the flow chart by showing the necessary flow of processes done by CAD tool in VLSI Design.