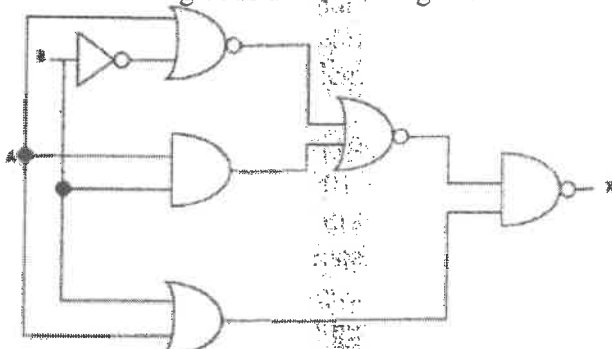


JK LAKSHMIPAT UNIVERSITY JAIPUR
INSTITUTE OF ENGINEERING AND TECHNOLOGY
End-Term Examination

Programme: B.Tech (ECE)
Course Name: DIGITAL SYSTEM DESIGN
Maximum Marks: 30

Year/Semester: 2023/3rd sem
Course Code: EE1110
Time Allowed: 2:30 Hours

- All questions are compulsory.
- The student, before starting to write the solutions, should please check the question paper for any discrepancy and ensure that they have been delivered the question paper of right course code.

Sr. No.		Question	Marks	CO
1.		You need to design a synchronous sequential circuit in the form of a positive edge-triggered Moore machine. The input signal w is synchronized with the clock pulses C. The output signal z should become 1 each time the value of the input signal w had not changed for two clock pulses. This change in the output value will appear at the clock pulse following the two pulses with the identical w values. See the example below for clarification. w: 00110001101110011111000010110 ... z: 001010100100100101000001000001 ... a) Set up the circuit's state table and draw the state diagram. b) Use the binary code to encode the states and set up the encoded state table. Obtain the minimized expressions for the next state and the output functions. No schematic of the circuit needs to be drawn.	3+3	5
2		For a Digital circuit discuss the importance of SETUP and HOLD Time with timing diagram?	3+3	3
3	a	Construct a 3-bit synchronous Up/Down counter using T Flip Flop. Draw the circuit and Timing diagram neatly.	3	1
	b	Design and Explain BCD adder	3	1
4.	a	Write a behavioral Verilog code for following ckt: 	3	2
	b	Design a 4 bit Asynchronous D FF in Verilog HDL and draw the expected output waveform. Mention comments for each Verilog command.	3	2
5	a	Inside an FPGA discuss how data is routed through an FPGA chip?	3	4
	b	You are supposed to configure a FPGA board. How would you do this? Can you do it in multiple ways? If yes, what different options you have and how are these options different from one another.	3	4