

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), Nov.-Dec. 2015

B. Tech in Computer Science Engineering, Semester VII

Roll No.....

CSE733: Parallel Processing

Time: 3 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A	Objective type multiple choice questions (10 questions @ 1 mark)	10
i.	Multi-computers are – a) Distributed address space accessible by local processors b) Simultaneous access to shared variables can produce inconsistent results. c) Requires message filtering for more than 1 computer. d) Share the common memory.	
ii.	Multi-Processors are – a) Share the common memory. b) Systems contain multiple processors on a single machine. c) Consists of a number of processors accessing other processors. d) Multiprocessor implementation for Non-embedded systems.	
iii.	SIMD computers are – a) Computer consists of limited identical processors. b) A modern supercomputer is almost always a cluster of MIMD machines c) Single instruction with multiple data. d) General instruction in computer.	
iv.	Program Partitioning and Scheduling Lines are defined as those lines which are coplanar and do not intersect, is the Condition of – a) Partitioning b) Parallelism. c) Scheduling d) Multiprocessing	
v.	VLSI stands for – a) Very Large Scale Integration b) Variable length serial mask. c) Virtual limit of sub interface. d) Very last stack instruction.	
vi.	Hierarchical memory system technology uses – a) Cache memory b) Memory sticks. c) Hdd. d) Virtual memory.	

vii.	In which of the following order of program execution explicitly stated in user programs? a) Program Flow Mechanisms b) Control Flow mechanism c) Data Flow mechanism d) Reduction flow mechanism	
viii.	Shared memory, program counter, control sequencer are features of - a) Data Flow b) Program Flow c) Control Flow mechanism d) Reduction flow mechanism	
ix.	APT is - a) Advanced processor technology b) Advertise poster trend. c) Addition part of tech. d) Actual planning of tech.	
x.	The crossbar switch was most popular from - a)1950 to 1980 b)1980-2000 c)1970-1990 d)1960-2000	

Q.2	Short answer type questions (4 questions @ 2.5 marks)	10
a.	Differentiate serial and parallel computation	
b.	Discuss authentication feature of web servers.	
c.	Why IPSec protocol is required?	
d.	Explain locality of reference concept.	

Q.3A	Discuss the usability of Grid and Cloud with respect to service application. Illustrate principle behind Cloud Computing and Grid Computing.	05
Q.3B	How P2P computing applications exist, focusing file sharing, process sharing and collaborative environments?	05

Q.4A	Explain importance of web server map the path component of Uniform Resource Locator.	05
Q.4B	Explain the conditions for partitioning and parallelism with example.*	05

Q.5A	Describe taxonomy of Parallel Processor Architectures for SIMD and MIMD.	05
Q.5B	How do processes exchange information in shared-memory architectures and distributed-memory architectures?	05

Q.6A	Consider the following loop: for (i=0; i<5000; i++) {job(i)} that is executed in an MIMD architecture. Processing time for job(i) is 30 microseconds. If Job(i) is executed on a 6 processing segment pipeline with each segment requiring 5 microseconds, what is the speed up achieved?	05
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Q.6B	Explain Flynn's classification with pseudocode.	05
	OR	
Q.6B	Elaborate Symmetric multi-processor organization in detail and mention 3 advantages with explanation.	05
Q.7A	CC-NUMA architectures logically follow in scaling from symmetric multiprocessing (SMP) architectures. Illustrate. Discuss CC-NUMA architecture in detail.	05
Q.7B	Differentiate workstation and cluster using appropriate example.	05
	OR	
Q.7B	Explain the utility of Hybrid Multi-processor by considering real time application.	05
Q.8	Discuss the importance of Backfilling mechanism. Describe Backfilling approach in scheduling task of parallel processing. Explain two types of backfilling approaches used in parallel approach.	10
Q.9A	Read the case study given below and answer the questions given at the end. The key to higher performance in microprocessors for a broad range of applications is the ability to exploit fine-grain, instruction-level parallelism. Some methods for exploiting fine-grain parallelism include:1. Pipelining2. Multiple Processors3. Superscalar implementation4. Specifying multiple independent operations per instruction. Pipelining is now universally implemented in high-performance processors. Little more can be gained by improving the implementation of a single pipeline. Using multiple processors improves performance for only a restricted set of applications. Superscalar implementations can improve performance for all types of applications. Superscalar means the ability to fetch, issue to execution units, and complete more than one instruction at a time. Superscalar implementations are required when architectural compatibility must be preserved, and they will be used for entrenched architectures with legacy software, such as X 86 architecture that dominates the desktop computer market. Specifying multiple operations per instruction creates a very-long instruction word architecture or VLIW. AVLIW implementation has capabilities very similar to those of a superscalar processor—issuing and completing more than one operation at a time—with one important exception: the VLIW hardware is not responsible for discovering opportunities to execute multiple operations concurrently. For the VLIW implementation, the long instruction word already encodes the concurrent operations. This explicit encoding leads to dramatically reduced hardware complexity compared to a high-degree superscalar implementation of a RISC or CISC. The big advantage of VLIW, then, is that a highly concurrent (parallel) implementation is much simpler and cheaper to build than equivalently concurrent RISC or CISC chips. VLIW is a simpler way to build a superscalar microprocessor. 1. Why do we need VLIW Architecture? 2. Discuss Software instead of Hardware implementation advantages of VLIW.	10

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