

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), April- May 2016
B. Tech. in Computer Science and Engineering, Semester IV

Roll No.....

CSE403: COMPUTER ARCHITECTURE AND
ORGANIZATION

Time: 03 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. * Use of CALCULATOR is not allowed

Q.1A Objective type multiple choice questions (10 questions @ 1 mark)

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- i. In a virtual memory system, the addresses used by the programmer belongs to
(A) Memory space. (B) Physical addresses.
(C) Address space. (D) Main memory address.
- ii. The I/O processor has a direct access to and contains a number of independent data channels.
A) main memory B) secondary memory C) cache D) flash memory
- iii. The techniques which move the program blocks to or from the physical memory is called as _____.
a) Paging b) Virtual memory organization
c) Overlays d) Framing
- iv. When the CPU detects an interrupt, it then saves its
A) Previous state B) Next state C) Current state D) Both A and B
- v. The main purpose of having memory hierarchy is to
A) Reduce access time B) Provide large capacity
D) Reduce propagation time D) Both a and b
- vi. The transformation between the Parallel and serial ports is done with the help of _____.
A) Flip flops B) Shift registers
C) Logic circuits D) None of the above
- vii. The technique where the controller is given complete access to main memory is
A) Cycle stealing B) Memory stealing
C) Memory Con D) Burst mode
- viii. The advantage of I/O mapped devices to memory mapped is
a) The former offers faster transfer of data
b) The devices have to deal with fewer address lines
c) The devices connected using I/O mapping have a bigger buffer space
d) No advantage as such
- ix. Devices that are used primarily to transport data between the processor and the



user are known as

A) Networking devices

B) Basic storage devices

C) Data presentation device

D) Data transfer device

- x. The best mode of connection between devices which need to send or receive large amounts of data over a short distance is _____.

A) Parallel Port

B) Serial port

C) BUS

D) Isochronous port

Q.2 Short answer type questions (4 questions @ 2.5 marks)

10

- i. What is the role of cache memory in pipeline?
- ii. What is an I/O interface?
- iii. In a cache with 64-byte cache lines how many bits are used to determine which byte within a cache line an address points to?
- iv. Differentiate between computer architecture and computer organisation?

Q.3A Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:
(a) 01101101 (b) 11111101

05

Q.3B What do you mean by software and Hardware interrupts? How these are used in microprocessor.

05

Q.4A The access time of a cache memory is 120 ns and that of main memory 900 ns. It is estimated that 80% of the memory requests are for read and remaining 20% for write. The hit ratio for read access only is 0.9. A write-through procedure is used.

05

(i) What is the average access time of the system considering only memory real cycles?

(ii) What is the hit ratio taking in to consideration the write cycle?

(iii) What is the average access time of the system for both read and write requests.

Q.4B Differentiate between synchronous and asynchronous bus.

05

Q.5A Using 8-bit 2's complement representation of negative numbers, perform the following computations:

05

(i) $-35 + (-11)$ (ii) $19 - (-4)$

Q.5B What is an I/O processor? Briefly discuss.

05

OR

Q.5B A Hard disk with 5 platters has 2048 tracks/ platter, 1024 sector/track (fixed number of sector per track) and 512 byte sectors. What is its total capacity?

05

- Q.6A Differentiate among direct mapping and associate mapping in cache memory? 05
- Q.6B Explain in detail about memory Hierarchy with neat diagram? 05
- Q.7A (a) How many 128×8 RAM chips are needed to provide a memory capacity of 8192 bytes? 05
 (b) How many lines of the address bus must be used to access 2048 bytes of memory? How many these lines will be common to all chips?
 (c) How many lines must be decoded for chip select? Specify the size of decoder.
- Q.7B What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory. 05
- OR
- Q.7B What is the difference between isolated mapped I/O and memory mapped I/O. What are the advantages and disadvantages of each? 05
- Q.8A Write a short note on: (any two) 10
 (A) Parallel computing
 (B) Distributed computing
 (C) Serial and parallel interface
- Q.8B What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, cost and application? 05
- OR
- Q.8B What are various types of associative memory and its advantages and disadvantages? 05
- Q.9A Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals. 10
- Q.9B What are various buses and why they are need and how they work? 05
- OR
- Q.9B What is the difference between serial and parallel transfer? Explain with the required example. 05

