

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), April-May 2015

M. Tech in Electronics & Communication Engineering, Semester II

Roll No.....

MTEC203: VLSI DESIGN

Time: 3 hours

Max. Marks: 100

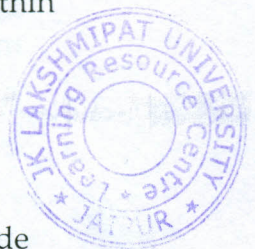
Instructions to students:

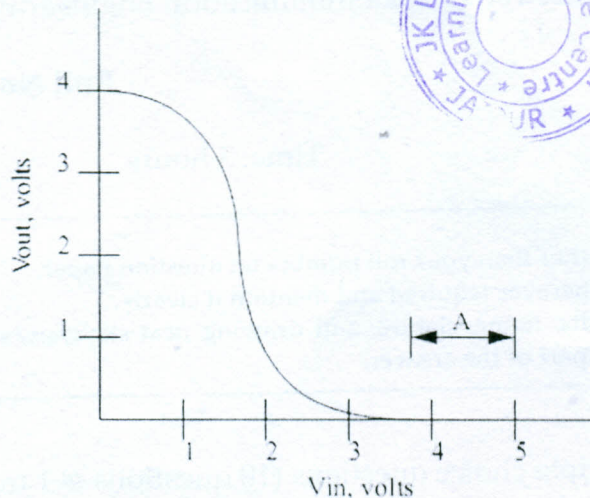
1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A Objective type multiple choice questions (10 questions @ 1 mark)

10

- i. Which of the following is a disadvantage of using high-level metals within primitive cells?
 - a) higher transistor packing density
 - b) more metal layers needed for complete chip layout
 - c) less chip area required for routing
 - d) less resistance between cells
- ii. A nMOS transistor will have a collection of positive charges under the gate oxide during:
 - a) accumulation
 - b) depletion
 - c) inversion
 - d) all of the above
- iii. Which of the following is a reason why silicon CMOS circuits dominate the IC industry?
 - a) can get more CMOS gates in same chip area
 - b) CMOS gates are faster than any other logic structures
 - c) silicon is an expensive material
 - d) CMOS physics is complex to understand
- iv. To achieve equal pullup and pulldown times in a CMOS inverter, the P device is usually several times wider than the N device. What is the main reason for this?
 - a) Hole mobility is greater than electron mobility
 - b) Electron mobility is greater than hole mobility
 - c) The P threshold is greater than the N threshold
 - d) The N threshold is greater than the P threshold
- v. Consider the following voltage transfer curve for a CMOS inverter made from n-channel MOSFETs with a threshold of 1V and from p-channel MOSFETs with a threshold of -0.5V. Each threshold was measured with $V_{sb}=0$ for each MOSFET.





When the inverter has reached a steady state and is operating in the region marked "A" above, the

- pulldown is in the saturated region, and the pullup is off.
- pulldown is in the linear region, and the pullup is off.
- pulldown is in the linear region, and the pullup is in the linear region.
- pulldown is in the linear region, and the pullup is in the saturated region.
- not enough information to tell.

Check whether the given statements are True or False:

- A transmission gate is formed by placing an nMOS transistor in series with a pMOS transistor and connecting both inputs to a select/control signal.
- Propagation delay describes the time it takes for the input to rise from a low value to a high value.
- Two series switches controlled by A and B form the function A OR B.
- The maximum output voltage from a pMOS transistor with its Source connected to V_{DD} will be $V_{DD} - |V_{tp}|$.
- In a CMOS inverter, when the input is logic-high, the pMOS device is ON and the nMOS device is OFF.

Q.2 Short answer type questions (4 questions @ 2.5 marks)

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- What is latch-up in CMOS?
- Why do we need isolation between MOS transistors fabricated on a single chip?
- Show that the power density does not change in a device scaled using constant field scaling.
- Define propagation delay and derive expression for T_{PHL} for CMOS Inverter.

Attempt ANY Five from Q.3-Q.9

[5 * 6M = 30M]

- Draw two-input CMOS NOR gate and obtain expression for switching threshold voltage (V_{th}). Assume that both NMOS transistors are identical. Similarly, PMOS transistors are also identical. 06
- Draw the CMOS Inverter circuit and Voltage Transfer Characteristic (VTC) for different operating regions of the nMOS and pMOS transistors. 06
- Explain the Short Channel Effects on threshold voltage and mobility of the charge carriers. 06

- 6 Discuss following approaches (with examples) used to reduce complexity of IC design: 1. Hierarchy, 2. Regularity, 3. Modularity, and 4. Locality 06
- Q.7 Write a short note on CMOS transmission logic gate. 06
- Q.8 Realize the following Boolean function using CMOS ratioded logic. 06
- $$F = AB + A'C' + AB'C.$$
- Q.9 Prove $(W/L)_p \approx 2.5 (W/L)_n$ for CMOS inverter. Assume suitable parameters value 06
- Q.10 Write the short note on: (Attempt ANY TWO) 10
- Channel length modulation
 - Constant field scaling
 - Constant voltage scaling
 - Data flow model in HDL
- Q.11 Draw circuit of resistive load inverter. Derive V_{IH} , V_{IL} , V_{OL} and V_{OH} for resistive load inverter. 10
- Q.12 Explain switching power dissipation in CMOS Inverter circuit. Assume ideal step as an input to CMOS Inverter. Under what constraints, derived expression can be applied to any CMOS logic circuit? 10
- OR**
- Draw input and output waveforms during high to low transition of output for a CMOS inverter. Derive expression for τ_{PHL} .
- Q.13 Consider a CMOS Inverter circuit with the following parameters: 10
- $V_{DD}=3.3V$, $V_{TO,n}=0.6V$, $V_{TO,p} = -0.7V$, $k_n=200 \text{ A/V}^2$, $k_p=80 \text{ A/V}^2$
- Calculate the noise margin of the circuit.
- OR**
- Design a resistive load inverter with $R = 1k\Omega$, such that $V_{OL} = 0.6V$.
The enhancement type nMOS driver transistor has the following parameters:
 $V_{DD} = 5.0V$, $V_{TO} = 1.0 \text{ V}$, $\gamma = 0.2 \text{ V}^{1/2}$, $\lambda = 0$, $\mu_n C_{ox} = 22.0 \mu\text{A/V}^2$
- Determine the required aspect ratio, W/L .
 - Determine V_{IL} and V_{IH} .
- Q.14 Explain switching power dissipation in CMOS Inverter circuit. Assume ideal step as an input to CMOS Inverter. Under what constraints, derived expression can be applied to any CMOS logic circuit? 10
- OR**
- Draw input and output waveforms during high to low transition of output for a CMOS inverter. Derive expression for τ_{PHL} .

