



JK LAKSHMIPAT UNIVERSITY JAIPUR
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/Backlog), Nov-Dec 2016
B. Tech. in Electronics & Comm. Engineering, Semester - VII

Roll No.....

ECE728: VLSI DESIGN (Elective)

Time: 3 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A	Objective type multiple choice questions (10 questions @ 1 mark)	10
i.	In present day VLSI circuit realization, power has become an important issue because of (a) transistor count is increasing (c) greater device leakage currents (b) higher speed of operation (d) All of the above	
ii.	In bulk CMOS technology, the substrate used for fabricating MOS transistor is _____. (a) an insulator (b) lightly doped p-type/ n-type (c) heavily doped p - type/ n-type (d) none of the above	
iii.	The noise margin for CMOS technology in comparison to Bipolar technology is High (b) Low (c) equal (d) exactly half	
iv.	An pMOS transistor is almost a perfect switch in (a) passing "1" only (b) passing "0" only (c) passing both "1" and "0" (d) cannot pass any of them	
v.	When the channel is implanted, then the MOS transistor is said to be operated in _____. (a) Depletion mode (b) enhancement mode (c) Non Saturated mode (d) Saturated mode	
vi.	How many architecture can be associated with an entity? (a) only one (b) two (c) three (d) none	
vii.	If L is the length of the channel & μ as the mobility of electron/hole , then the electron transit time can be expressed as $\frac{\mu V_{ds}}{L^2}$ (b) $\frac{L^2}{\mu V_{ds}}$ (c) $\frac{L^2}{\mu V_{gs}}$ (d) $\frac{\mu V_{gs}}{L^2}$	
viii.	Transmission gate is a restoring device (a) TRUE (b) FALSE	
ix.	For CMOS NAND gate with increase in fan-in, the inversion voltage (a) Remains unaffected (b) moves towards left (c) moves towards right (d) moves up and down	

x.	In VHDL , a digital system is modelled as (a)Module (b) entity (c) process (d) all of the above	
Q.2	Short answer type questions (4 questions @ 2.5 marks)	10
i.	Distinguish between energy & power dissipation of VLSI circuits. How power dissipation is related to the reliability of a VLSI circuit?	
ii.	What are the three regions of operation of MOS transistor?	
iii.	State the basic differences between nMOS & pMOS transistors.	
iv.	Sketch a transistor-level schematic for a CMOS 4-input NOR gate. Explain it briefly and give the truth table.	
Q.3A	What is latch up problem that arises in bulk CMOS technology? How it can be overcome?	05
Q.3B	What is body effect? How it influences the threshold voltage of a MOS transistor?	05
Q.4A	With a suitable diagram explain function of an nMOS Inverter. Mention its transfer characteristics also.	05
Q.4B	Make a proper comparison between CMOS & Bi-polar technology.	05
Q.5A	Define the tri state buffer, tri state inverter and transmission gate. Draw their symbol and also the truth table.	05
Q.5B	What is a Multiplexer? Sketch 2:1 CMOS multiplexer and explain briefly.	05
Q.6A	Use the combination of CMOS gates to generate the functions from A,B, and C such as $Y = A\bar{B} + \bar{A}B$.	05
Q.6B	Sketch a transistor-level schematic for a CMOS 4-input NOR gate. Explain it briefly and give the truth table.	05
	OR	
Q.6B	What are pass transistors? State and explain the pull-up to pull-down ratios for inverting logic coupled by pass transistors.	05
Q.7A	For the function $\bar{F} = (X + Z).(\bar{X} + \bar{Z}).\bar{Y}$, give the complete VHDL Design.	05
Q.7B	Outline the benefits of SOI technology in comparison to conventional bulk CMOS technology.	05
	OR	
Q.7B	What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?	05
Q.8A	Step by step procedures are adopted for the fabrication of nMOS. With a suitable diagrams explain the procedure in detail.	10
Q.9A	Outline the various processes used for the fabrication of CMOS. Explain the in detail the p-well process with suitable diagram.	10
Q.9B	Develop the complete VHDL design for (a) 2-to-1 MUX. (b) Full Subtractor	10
	OR	
Q.9B	Show that the relation between drain to source current (I_{ds}) vrs Voltage (V_{ds}) for a typical MOS transistor is given as $I_{ds} = C_o \mu \frac{W}{L} ((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2})$; All the symbols have their usual meanings.	10

.....Best of Luck.....