

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), May 2022
BTech CSE, Semester IV

Roll No.....

CS1107: Computer Architecture and Organization

Time: 3 hours

Max. Marks: 60

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

Q.1	Design a memory with the size of 4096 Bytes (4096×8). Half of the memory should be design with the help of RAM chip and rest half with the help of ROM chip. The size of RAM chip is 512 Byte (512×8) and size of ROM chip is 1024 Byte (1024×8). Find the number of RAM and ROM chip required. Also draw the memory address map and CPU to Memory interfacing diagram.	08 (CO5)
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Q.2	Consider the main memory have three page frames (0,1,2). Processor requires the pages from the virtual memory in the following order 6, 7, 8, 9, 6, 7, 1, 6, 7, 8, 9, 1. Show and Compare the implementation of FIFO, LRU and LFU. also calculate Hit ratio in each case.	08 (CO9)
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Q.3	In cache mapping, the size of main memory is 4GB and size of cache memory is 8KB. Where each location the data is of 8 bits or 1 Byte. And each block contains the 32 B locations. a) Find the total number of bits required for addressing the main memory. b) How many bits are required to represent TAG, Block number and locations for One way, Two Way and Four way set associative mapping. Which one in part b) will be the better for the overall computing process. Justify your answer.	08 (CO8)
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Q.4	In virtually all systems that include DMA modules, DMA access to main memory is given higher priority than the processor access to main memory. Why?	06 (CO7)
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Q.5	A DMA module is transferring characters to memory using cycle stealing, from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity? Assume 8 bits per character.	10 (CO4)
Q.6	Consider the sequence of machine instructions given below: <pre>MUL R5, R0, R1 DIV R6, R2, R3 ADD R7, R5, R6 SUB R8, R7, R4</pre> In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: - Instruction Fetch and Decode (IF), - Operand Fetch (OF), - Perform Operation (PO) and - Write back the Result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instructions?	16 (CO8)
Q.7	Write initialization instructions for the 8255A to be set up - Port A as output port in mode 0 - Port B as an output port in mode 0 for interrupt I/O - Port C_U as an output port in mode 0	04 (CO4)