

# JK LAKSHMIPAT UNIVERSITY, JAIPUR

## INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term, Theory Even Semester, Special Examination (Backlog), December 2015

B. Tech in Electronics and Communication / Electrical Engineering, Semester VI

Roll No.....

ECE 622 / EE 622: MICROPROCESSORS AND  
INTERFACING

Time: 3 hours

Max. Marks: 100

---

### Instructions to students:

1. Do not write anything other than your roll number on question paper.
  2. Assume suitable data wherever required and mention it clearly.
  3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
- 

Q.1A Objective type multiple choice questions (10 questions @ 1 mark) 10

- i. In which T-state the ALE signal is activated in an 8085 microprocessor timing cycle? (a) T1 (b) T2 (c) T3 (d) T4.
- ii. RST 6.5 is a (a) Non-vectored Interrupt (b) vectored Interrupt (c) a simple I/O pin (d) none of these.
- iii. Which mode of 8255 is bidirectional? (a) 0 (b) 4 (c) 2 (d) 1
- iv. How many address lines are used in the Memory mapped I/O interfacing scheme? (a) 10 (b) 12 (c) 8 (d) 16.
- v. IC 2716 is a (a) 2Kx8 ROM (b) 8Kx8 ROM (c) 4Kx8 RAM (d) 16Kx8 ROM
- vi. To start the entire system which signal is used by 8085? (a) RESET OUT (b) READY (c) CLK OUT (d) INTA'.
- vii. Find the odd man out (a) CMC (b) ANA (c) INX (d) RAL.
- viii. A buffer is used to interface a /an ----- device (a) Input (b) Output (c) Memory (d) Programmable
- ix. EPROM is generally erased by using (a) Ultraviolet rays (b) infrared rays (c) 12 V electrical pulse (d) 24 V electrical pulse.
- x. The no. of address lines required to address a memory of size 16 K is (a) 15 lines (b) 16 lines (c) 18 lines (d) 14 lines

Q.2 Short answer type questions (4 questions @ 2.5 marks) 10

Q.2A If the following program is executed, explain its effect when CY flag = 0 and 1.

MOV A,B

RAR

MOV B,A

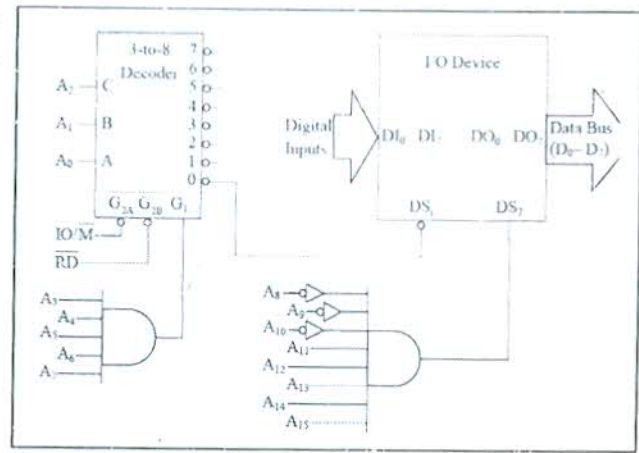
Q.2B Form the control word to set and reset the PC3 and PC7 pins of 8255.

Q.2C Form the control word for 8255A for the following conditions: Port A = Mode 2 (output); Port B = Mode 1 (input), Port C<sub>lower</sub> = input and Port C<sub>upper</sub> = output.

Q.2D Given an 8-bit ADC with V<sub>REF</sub> = 10 volts. What will be the value of LSB and how many output codes are possible.

- Q.3A With a neat sketch, draw the Opcode Fetch machine cycle timing diagram of the instruction MOV D,C. This is a 1-byte (51h), 1-machine cycle and 4T-state instruction. Assume that the opcode is stored in the memory location 2501h. 05
- Q.3B An 8085 instruction LDA 2502h loads the 8-bit contents of the memory location 2502h into the accumulator register. The hex code (opcode) for this instruction is 3Ah. Identify the no. of bytes, the machine cycles with their names and the no. of T-states in this instruction. If the 8085 is operating at a frequency of 3 MHz, then what will be the total execution time for this instruction? 05
- Q.4A Describe briefly the addressing modes available in 8085 microprocessor (by giving suitable examples, use single sentence for each case). 05
- Q.4B Draw only the flow-chart to find a number with maximum value in a series of 10 bytes stored from memory location 2300h. The result must be stored at the memory location 2500h. 05
- Q.5A Write a program to multiply 10 numbers by 4 which are stored from memory location 2400h and store the multiplied values from memory location 2500h onwards. (**Restriction:** use only register pairs as memory pointers) 05
- Q.5B Define the following terms using single sentence for each: Assembly Language, Machine Language, Instruction Cycle, Machine Cycle and T-state. 05
- Q.6A Write a program to find the number of negative numbers among the 10 numbers stored from memory location 2001 onwards. The result should be stored in the memory location 2500h. (**Restriction:** use only register pairs as memory pointers) 05
- OR
- Q.6B Write a short assembly language program, without using any arithmetic instruction to store A6h in the flag register of 8085 microprocessor. Data in other registers of the processor must not alter upon executing this program. 05
- Q.7A An SRAM memory chip of size 8kx8 has been mapped to act both as ROM and RAM. The starting address of the chip is 2000h. The upper half is mapped as ROM whereas the lower half is mapped as RAM. (a) Show the addresses for both the halves (b) Design the write protection circuit needed. 05
- Q.7B If the control register of 8255 has been programmed as 88h, identify all the port configurations. Show the circuit to generate the base address as 50h, with all the addresses for respective ports and control register. 05
- OR
- Q.7B What do you understand by Linear and Absolute decoding techniques for interfacing of memory devices? Give a brief description of "Fold back Memory" concept with an example. 05

Q.8 The interfacing circuit of an I/O device is shown in the adjacent figure (Where  $DS_1$  and  $DS_2$  are the chip select signals). Assume negligible gate delays.



(a). Identify the address of the I/O device.

(b). Which operation the I/O device is performing?

(c). In which I/O mapping scheme the I/O device is mapped?

(d). If the AND gate at  $DS_2$  is connected at  $G_1$  by removing the AND gate at  $G_1$ , how the address of the I/O device will change?

(e). If the I/O device is replaced with a memory chip of  $4K \times 8$  and connected to a circuit obtained by connecting the input lines of the decoder C, B and A to  $A_{14}$ ,  $A_{13}$  and  $A_{12}$  respectively, whereas the  $A_{15}$  line to  $G_1$ , what will be the memory map (starting and ending addresses)? All the NAND gates are removed. Assume the output  $O_2$  of the decoder is connected to the chip select ( $CS'$ ) signal of the memory device.

Q.9 Design an interfacing circuit to interface two ROM chips and two RAM chips along with one 8255. The size of the ROM chips is  $4K \times 8$  while the size of the RAM chips is  $8K \times 8$ . The 8255 uses I/O Mapped I/O addressing scheme. You should use a 74LS138 decoder and minimum number of logic gates as needed for your design and label the signals properly. For getting partial marks show the following:

20

(a) Address maps for all the devices i.e. starting and ending addresses. (6 + 4 + 2 = 12 Marks)

(b) Interfacing circuit for the given problem. (8 Marks)

\*\*\*\*\*ALL THE BEST\*\*\*\*\*