

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination, July – Nov. 2016 (Backlog)

B. Tech. in Electronics & Communication Engineering, Semester IV

Roll No.....

ECE402: DIGITAL ELECTRONICS

Time: 3.0 hours Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
 2. Assume suitable data wherever required and mention it clearly.
 3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
 4. Use of Non-Programmable calculator is allowed.
-

Q.1A Objective type multiple choice questions (10 questions @ 1 mark)

10

- i. In which of the following base systems DEF is a valid number?
 - a. Base 10
 - b. Base 16
 - c. Base 8
 - d. Base 3
- ii. Storage of 1 GB means the following number of bytes
 - a. 1000 KB
 - b. 964 KB
 - c. 1024 KB
 - d. 1064 KB
- iii. The binary code of $(21.125)_{10}$ is
 - a. 10101.001
 - b. 10100.001
 - c. 10101.010
 - d. 10100.111
- iv. How many Flip-Flops are required for mod-8 counter? a. 5 b. 6 c. 2 d. 3
- v. A NAND gate is called a universal logic element because
 - a. it is used by everybody
 - b. any logic function can be realized by NAND gates alone
 - c. all the minimization techniques are applicable for optimum NAND gate realization
 - d. many digital computers use NAND gates.
- vi. A ring counter consisting of seven Flip-Flops will have states
- vii. The device which changes from serial data to parallel data is a. Counter b. MUX c. DEMUX d. Flip-flop
- viii. The information in ROM is stored a. By the user any number of times. b. By the manufacturer during fabrication of the device. c. By the user using ultraviolet light. d. By the user once and only once

- ix. A 4-bit synchronous counter uses flip-flops with propagation delay times of 25 ns each. The maximum possible time required for change of state will be a. 15 ns. b. 25 ns. c. 45 ns. d. 60 ns.
- x. What is the output frequency of a MOD 16 counter if the input frequency is 116 MHz?

Q.2 Each Question is of 2.5 marks

10

- I. Write the difference between RAM and ROM.
- II. Perform the following division in Binary $111011 \div 101$.
- III. Why do we use K Method?
- IV. Explain the significance of Course Digital Electronics.

- Q.3A i. What will be the 8 bit 2's complement representation of decimal number (-44). 05
- ii. Assume the number $(10011001)_2$ in 2's complement representation. What will be the decimal equivalent of the number?

- Q.3B A number of 256×8 bit memory chips are available. To design a memory organization of $2 \text{ K} \times 8$ memory. Identify the requirements of 256×8 memory chips and explain the details. 05

- Q.4 Add and multiply the following numbers without converting them to decimal. 10
- a. Binary numbers 1011 and 101
 - b. Hexadecimal numbers 2E and 34.

OR

- Q.4 Design a 4-bit SISO Register. How many clock pulses are required for Data IN and OUT? 10

- Q.5A Draw the original state diagram for the following input output sequences. Also reduce the number of states in that diagram and draw the reduced state diagram. 07

state	a	a	b	c	d	e	d	d	e	d	e	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

- Q.5B Simplify the following three variable expression using Boolean Algebra: 03
- $$Y(A,B,C) = \sum m(1,3,5,7)$$

- Q.6 I. Design a 2 bit comparator using suitable decoder. 05+05
- II. Using signed 2's complement perform the following
- a. $(+29) + (-49)$
 - b. $(-29) + (-49)$

- Q.7 Design a combinational circuit using a ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. 10

Also write the ROM dimensions.

Q.8A A digital system has a clock generator that produces pulses at a frequency of 80MHz. Design a circuit that provides a clock with a cycle time of 50 ns. 03

Q.8B Implement the following two Boolean functions with a PLA: 07

$$F_1(A, B, C) = \sum(0, 1, 2, 4)$$

$$F_2(A, B, C) = \sum(0, 5, 6, 7)$$

$$F_3(A, B, C) = \sum(0, 3, 5, 7)$$

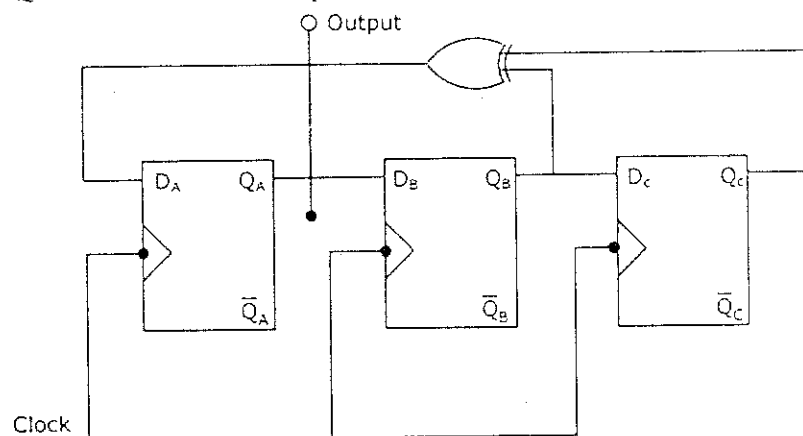
Q.9A Minimize the following expressions using K-map. 05

$$Y(A, B, C, D, E) = \sum m(1, 4, 6, 9, 10, 11, 14, 15, 23, 25, 31)$$

Q.9B Design a Asynchronous decade Counter using JK Flip Flops that counts from 0 to 5 sequence. 05

OR

Q.9B Assuming that flip-flops are in reset condition initially, the count sequence observed at Q_A for the four clock pulses in the circuit shown is 05



Q.10 A 4 bit number is represented by ABCD with D as LSB. Design a logic circuit that will produce a 1 whenever the input is greater than 0010 but less than 1000. Use minimum number of NAND gates. 10