

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/Backlog), November 2016

B. Tech. in Electronics & Communication Engineering, Semester VII

Roll No.....

ECE726: VHDL

Time: 3.0 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Non-Programmable calculator is allowed.

Q.1A	Objective type questions (10 questions @ 1 mark)	10
a.	In VHDL, which object/s is/are used to connect entities together for the model formation? a. Constant b. Variable c. Signal d. All of the above	
b.	Where is your design placed after it is compiled?	
c.	What are the names for the FPGA?	
d.	Which ieee standard is used for VHDL?	
e.	Give truth table for full subtractor.	
f.	How many types of modelling possible in VHDL? Name them.	
g.	How for loop is written in VHDL?	
h.	How switch case is used in VHDL?	
i.	What two clauses are required for the library part of a design entity in VHDL?	
j.	Is the following statement true or false? A complete process is a concurrent statement that is evaluated at the same time as another complete process or at the same time as other concurrent statements.	
Q.2	Each Question is of 2.5 marks	10
a.	What do you understand with state diagram?	
b.	Explain difference between SIGNAL and VARIABLE ?	
c.	Write a short note on behavioral modelling.	
d.	Write the truth table and expression for JK Flip Flop.	
Q.3A	Write the complete VHDL code for Memory Organization.	05
Q.3B	Write the complete VHDL code for LED Blinking.	05

Q.4A	Write a short note on a. Clock Synchronization b. CPU organization	05
Q.4B	Write the complete VHDL code for each of the following VHDL signal assignments in single code: a. $G1 \leq \text{not } A \text{ and } B \text{ or } C$ b. $G2 \leq A \text{ or } B \text{ exor not } C$	05
Q.5A	Show a complete VHDL design for a circuit that provides the 1's complement at its output for each 3-bit binary number applied at its input. Use the input signals X, Y, and Z and the corresponding output signals F1, F2, and F3.	05
Q.5B	Write the VHDL code for 4 bit BCD to Gray code convertor.	05
Q.6A	Write the VHDL code for Half Adder Circuit.	03
Q.6B	Explain and write the complete VHDL code for Bubble Sorting.	07
	OR	
Q.6B	Write the complete VHDL code for 4 bit multiplier circuit.	07
Q.7	Explain the serial adder circuit using Moore type FSM. Also write the complete VHDL code for this.	10
Q.8	Explain 8:4 divider algorithms and also write the complete VHDL code for this.	10
	OR	
Q.8	Explain 4 bit Shift Register algorithms and also write the complete VHDL code for this.	10
Q.9A	Draw the State diagram for the Vending Machine which has the following specifications. i. The machine takes quarters only (Q_i). ii. The machine can dispense: Water: 75 cents (W), Cola: 50 cents (C), Orange: 50 cents (B) iii. The machine has a Coin Return button (Cr) iv. Only one input may be active at a time v. Single product can be dispensed in one clock cycle vi. If more than 75 cents is inserted, the money is automatically returned vii. If no inputs are active, the state machine stays in the current state viii. Outputs: CRO: Coin Return Out (all money in the machine), Wo: Water Out, Co : Cola Out, Bo : Orange Out, Oo : Quarter Out	10
Q.9B	Write the VHDL for the Vending Machine in Q.9A	10