

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY
 End Term Examination (Regular/Backlog), May 2025
 BTech, Semester II

Roll No.....

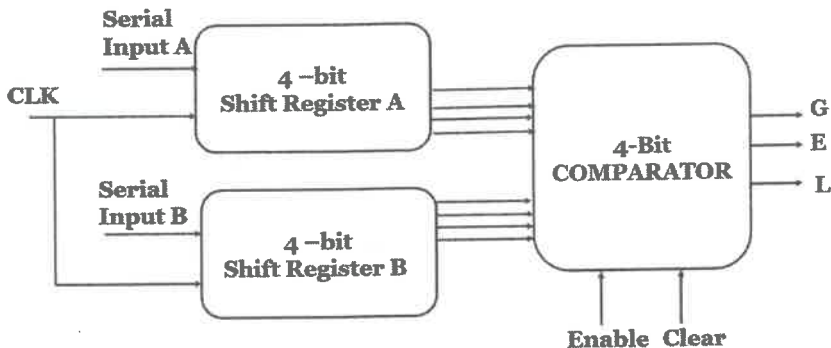
EE1120: Digital Circuit and Systems

Time: 2.5 hours

Max. Marks: 30

Instructions to students:

1. Do not write anything other than your roll number on the question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate nomenclature, and drawing neat schematics wherever required are an integral part of the answer.
4. Use of Programmable/Scientific Calculator is not allowed.

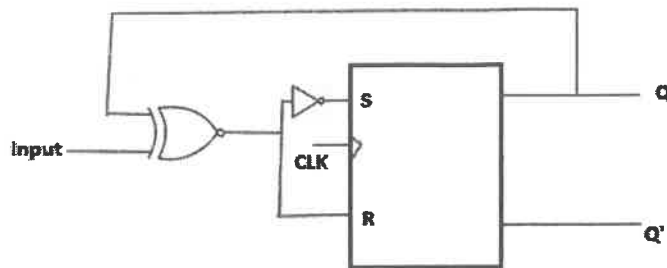
Q.1	What is the race-around condition in relation to J-K flip-flops? Explain how the race-around condition is eliminated in J-K flip-flops.	03(CO4)
Q.2	The diagram shows the application of Serial in Parallel Out shift registers where two registers A and B are used to store 4-bit binaries. The output of these registers is sent to a 4-bit comparator. Initially both the registers are in reset condition.  (A) Show the schematic diagram for one of these shift registers using D flipflops. Draw the timing diagram of the Shift Register A when decimal number 12 is being shifted to the adder. How many clock pulses are required to shift this number into the adder? (B) Enable a 4-bit comparator when the output of shift registers is ready. Show the schematic diagram of this comparator which has inputs A0 A1 A2 A3 from shift register A and inputs B0 B1 B2 B3 from shift register B. The output of the comparator should be G, E and L which should show the status $A > B$, $A = B$, $A < B$ respectively. Write the logical expressions for the three outputs and show the schematic diagram of the comparator. What modification is required in the logic circuit if we want to clear the output of the comparator after seeing the result?	03+03 (CO3,CO4)
Q.3	Design a synchronous down counter (3,2,1,0,3 and so on) using negative edge triggered JK Flip Flop.	04 (CO4)

Q.4

Consider the circuit shown in the figure below. Identify the type of flip-flop by drawing its characteristic table and excitation table. Also, write simplified Boolean expressions.

04

(CO2,CO4)



Q.5

The truth table and the graphical symbol for a mystery circuit are shown below. Implement this circuit using a 4-to-1 multiplexer and any number of basic logic gates (AND, OR, NOT). Assume that the input variables are available only in their regular (i.e., non-inverted form) as well as the constants 0 and 1. Label all inputs, outputs, and pins.

04

(CO2,CO3)

Truth table

S_1	S_0	A	B	y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Graphical symbol

Q.6

Design a state diagram and state table of FSM that detects if the previous two values of the input w were equal to 00 or 11. If either condition is true, then the output z should be set to 1; otherwise to 0.

04

(CO5)

Q.7

A pet shelter has taken in a new kitten. Two staff members, Ashley and Greg, have had trouble feeding her and have taken notes on when she won't eat. The kitten won't eat when neither Ashley nor Greg feed her, and she has had more than an hour of play time, and she gets fed Food-B (a type of cat food). When only Greg feeds the kitten, she won't eat unless she has an hour of play time and gets Food-B. When only Ashley feeds her, the kitten only eats if she has gotten an hour of play time, or she gets Food-B, but won't eat if both occur. When both Ashley and Greg feed her together, the kitten won't eat if she gets Food-B.

05

(CO2,CO3)

Use this information to fill out a truth table for the eating habits of this kitten and write down the minimize the expression. Clearly label all variables that your solution uses. The output function should be called E (short for Eat) and it should be equal to 1 if the cat will eat and 0 if it won't.