



JK Lakshmipat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End-Term Examination, May 26
B.Tech. Semester II

Roll No.....

EE1125: Digital Electronics

Time: 2.5 hours

Max. Marks: 30

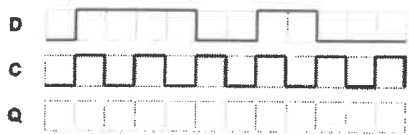
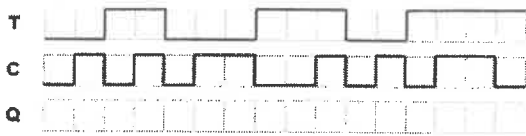
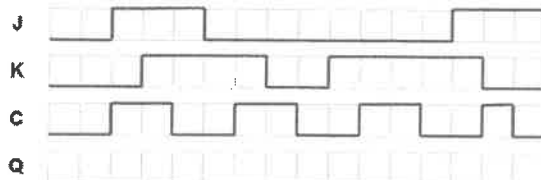
Instructions:

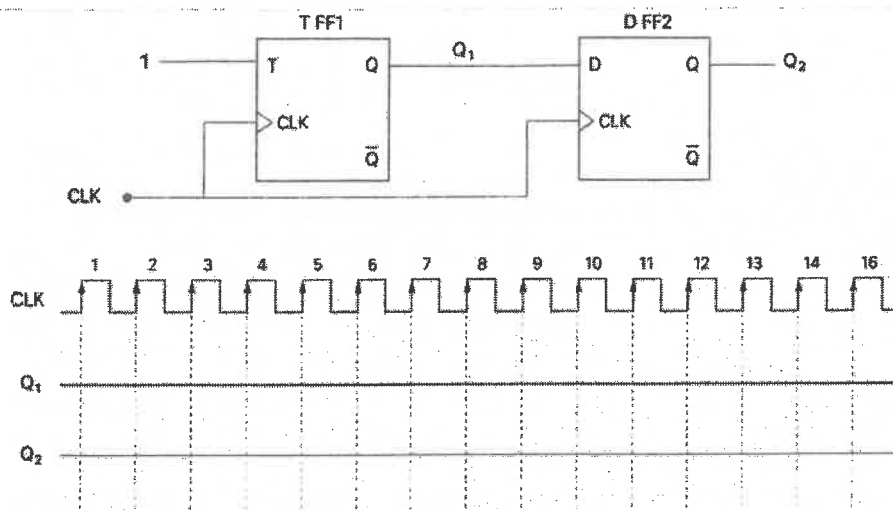
* Answer All.

* Calculator is not allowed.

Q.1.	1. Write the truth table for an even parity generator using 3 bits (X,Y,Z).	1.5 Marks
	2. Implement the Parity Generator using logic gates and show the schematic diagram.	1.5 Marks
	3. Implement the same function using 4:1 Multiplexer. Show the implementation table and the schematic diagram.	2 Marks

Q.2.	Implement the following given Boolean expressions using decoder: $F_1(A, B, C) = A'BC' + AC$ $F_2(A, B, C) = AB'C' + A'B$ $F_3(A, B, C) = A'B'C' + AB$	5 Marks
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Q.3.	Complete the timing diagrams for the specified flip-flops. In all the cases, the Clock signal is labeled C. You may assume that Q is initially at 0.	
	a. A negative-edge trigger D Flip-Flop (D-FF): 	1 Marks
	b. A positive-edge-trigger T Flip-Flop (T-FF): 	1 Mark
	c. A negative-edge-trigger J-K Flip-Flop (J-K FF): 	1 Mark
	d. Consider the following circuit: Draw the timing diagram for Q ₁ and Q ₂ . You may assume that Q ₁ and Q ₂ are initially at 0.	



2 Marks

Q.4. A Flipflop has two inputs A and B is having behaviour as follows:

5 Marks

- When $A=B=0$, next state is 0
- When $A=0, B=1$, state remain same
- When $A=1, B=0$, state gets complemented
- When $A=B=1$, next state is 1

Provide the required tables and the next state equation.

Q.5. Analyze the race around condition in a JK flip-flop and design a master-slave JK flip-flop to eliminate this problem and explain its operation with the help of a timing diagram.

5 Marks

Q.6. Design a synchronous counter using J-K flip-flops to generate the sequence 0, 1, 2, 3, 4, 0, ... and repeat.

5 Marks

- Draw the state diagram.
- Construct Excitation table.
- Draw the logic circuit using FF(s).
- Draw the output waveform.

*****All The Best*****