

JK Lakshmipat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/Backlog), April 2024
BTech, Semester II

Roll No.....

EE1120: Digital Circuit and Systems

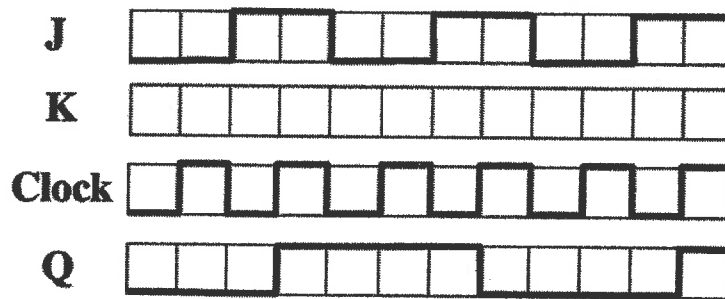
Time: 2.5 hours

Max. Marks: 30

Instructions to students:

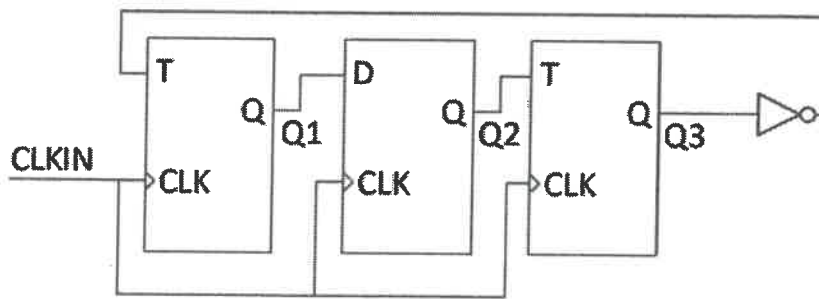
1. Do not write anything other than your roll number on the question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

Q.1	Use the theorems of Boolean Algebra to simplify the formula given below into a minimum cost expression. Draw the circuit diagram for the minimized expression using only NOR gates. $F(X,Y,Z)=XYZ'(X+Y)+Z'(X+Y')'+X(X'+YZ)'+(Z+XY')+(X'+Z)'$	03 (CO2, CO3)																																																																								
Q.2	The Boolean function $F(A,B,C,D)$ that is described as follows: The output of this function is 1 if the decimal representation of the 4-bit binary number ABCD is a non-zero even number. Otherwise, the output is equal to 0. Use the K-Map to derive the minimum POS expression for this function. Draw the circuit diagram for this function.	04 (CO2)																																																																								
Q.3	Complete the timing diagram for the specified flip-flop such that output Q will be as indicated. Assume that flip-flops are positive edge triggered flip-flops. If more than one value is possible for any input, indicate that with a don't care d. D <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Clock <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Q <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> T <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Clock <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Q <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>																																																																									03 (CO4)

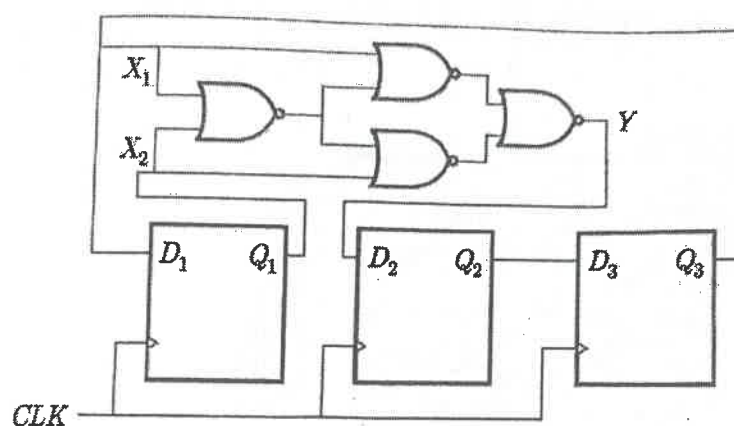


Q.4 Provide the state diagram only, with proper marking for Mealy Sequence Detector for sequence 1010. Draw state diagram for non-overlapping case and for the overlapping case. 03 (CO5)

Q.5 Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is the clock input to the circuit. At the beginning, Q1, Q2, and Q3 have values 0,1 and 1 respectively. Which values of Q1, Q2, and Q3 can NEVER be obtained with this digital circuit? Show all the proper outputs till you reach your final answer. There is no marks for a direct answer. 04 (CO4; CO5)



Q.6 Consider the circuit shown in the figure 01+03 (CO4, CO5)

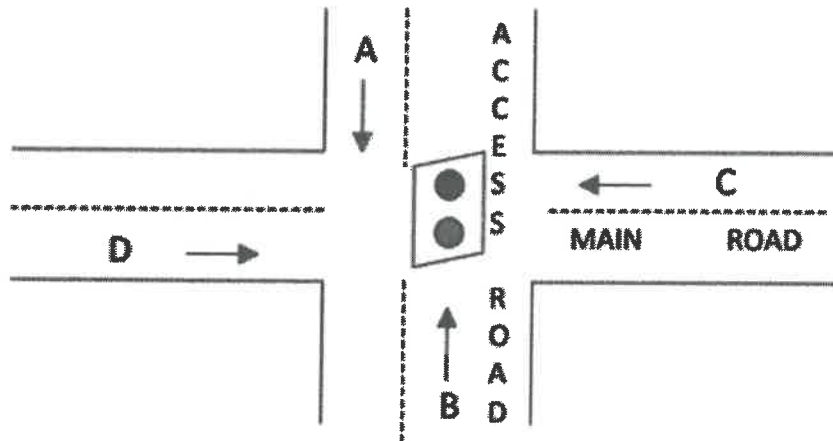


a. Calculate the correct input output relationship between Y and (X1, X2) in the form of single logic gate.

b. The D flip Flop are initialized with the $Q_1Q_2Q_3 = 000$, What will be the $Q_1Q_2Q_3$ after 1st, 2nd and 3rd clock. Show the proper steps.

Q.7 Design a MOD 8 (0 to 7 to 0...) asynchronous up Counter (using negative edge triggered JK FF). 04 (CO4)

Q.8 The given figure represents the intersection of a main highway with a secondary access road. Vehicle detection sensors are placed along lanes C & D (main road) and lanes A & B (access road). These sensor outputs are LOW when no vehicle is present and at least one sensor output is High when a vehicle is present. 05 (CO2, CO3)



The intersection traffic light is to be controlled according to following logic:

- The east-west(E-W) traffic light will be green whenever both lanes C and D are occupied.
- The E-W light will be green whenever either C or D is occupied but lanes A and B are not both occupied.
- The north-south(N-S) light will be green whenever both lanes A and B are both occupied but C and D are not both occupied.
- The N-S light will also be green when either A or B is occupied while C and D are both vacant.
- The E-W light will be green when no vehicles are present.

Using the sensor outputs A, B, C and D as inputs, design a logic circuit to control the traffic light. There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be green. Simplify the circuit using K map and draw the logic diagram.

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