



JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), Apr-May 2015

B. Tech. in Electronics & Communication Engineering, Semester IV

Roll No.....

ECE402: DIGITAL ELECTRONICS

Time: 3.0 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Non-Programmable calculator is allowed.

Q.1A Objective type multiple choice questions (10 questions @ 1 mark) 10

- i. In order to add these two binary number $1111 + 1101$. How many full and half adders required?
- ii. The minimum number of 2 input NAND gates required to implement the Boolean function $Z = AB'C$, assuming that A, B and C are available, is
 - A. Two
 - B. Three
 - C. Five
 - D. Six
- iii. The decimal equivalent of hex number 1A53 is (A) 6793 (B) 6739 (C) 6973 (D) 6379.
- iv. How many Flip-Flops are required for mod-16 counter? (A) 5 (B) 6 (C) 3 (D) 4
- v. EPROM contents can be erased by exposing it to
 - A. Ultraviolet rays
 - B. Infrared rays
 - C. Burst of microwaves
 - D. Intense heat radiations
- vi. A ring counter consisting of five Flip-Flops will have (A) 5 states (B) 10 states (C) 32 states (D) Infinite states
- vii. The device which changes from serial data to parallel data is (A) Counter (B) MUX (C) DEMUX (D) Flip-flop
- viii. The information in ROM is stored (A) By the user any number of times. (B) By the manufacturer during fabrication of the device. (C) By the user using ultraviolet light. (D) By the user once and only once
- ix. A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be (A) 15 ns. (B) 30 ns. (C) 45 ns. (D) 60 ns.
- x. What is the output frequency of a MOD 16 counter if the input frequency is 96 MHz?



Q.2 Each Question is of 2.5 marks

10

- I. Write the difference between DRAM and SRAM.
- II. Find the 9's and 10's complements of the following decimal numbers
 - a. 12345678
 - b. 63325600
- III. Why do we use QM Method to minimization of logic functions?
- IV. Explain the significance of Course Digital Electronics.

Q.3A A staircase light is controlled by two switches one at the top of the stairs and another at the bottom of stairs (i) Make a truth table for this system. (ii) Write the logic equation in SOP form. (iii) Realize the circuit using AND-OR gates. 05

Q.3B A number of 256×8 bit memory chips are available. To design a memory organization of $2 \text{ K} \times 8$ memory. Identify the requirements of 256×8 memory chips and explain the details. 05

Q.4A The following is a truth table of a three input, four output combinational circuit: 05

Inputs			Outputs			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

Tabulate the PAL programming table for the circuit and mark the fuse map in a PAL diagram

Q.4B Using signed 2's complement perform the following

05

$$(+29) + (-49)$$

$$(-29) + (-49)$$

OR

Q.4B Design a counter with the following repeated binary sequence: 0,1,2,3,4,5,6. Use JK flip flops. 05

Q.5A Draw the original state diagram for the following input output sequences. Also reduce the number of states in that diagram and draw the reduced state diagram. 07

state	a	a	b	c	d	e	d	d	e	d	e	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

Q.5B Design a 4-bit PISO Register. How many clock pulses are required for Data IN and OUT? 03

Q.6 Design a combinational circuits that generates 9's compliment and 10's compliment of a BCD digit 10

Q.7 Design a combinational circuit using a ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. Also write the ROM dimensions. 10

Q.8A A digital system has a clock generator that produces pulses at a frequency of 80MHz. Design a circuit that provides a clock with a cycle time of 50 ns. 03

Q.8B Implement the following two Boolean functions with a PLA: 07

$$F_1(A, B, C) = \sum(0, 1, 2, 4)$$

$$F_2(A, B, C) = \sum(0, 5, 6, 7)$$

$$F_3(A, B, C) = \sum(0, 3, 5, 7)$$



Q.9A Explain the Master-Slave D flip flop with suitable equations. 03

Q.9B Design a Asynchronous decade Counter using JK Flip Flops that counts from 0 to 9 sequence. 07

OR

Q.9B A binary ripple counter uses flip flops that trigger on the positive edge of the clock. What will be the count if 07

- I. The normal outputs of the flip flops are connected to the clock and
- II. The compliment outputs of the flip flop are connected to the clock
- III. What happens if negative edge of the clock is used to trigger counter flip flops.

Q.10 A sequential circuit has two JK flip flops A and B, two input x and y, and one output z. The flip-flop input equations and circuit output equation are 10

$$J_A = Bx + B'y'$$

$$K_A = B'xy'$$

$$J_B = A'x$$

$$K_B = A + xy'$$

$$z = Ax'y' + Bx'y'$$

- I. Draw the logic diagram the circuit.
- II. Tabulate the state table.
- III. Derive the state equation for A and B.