

JK Lakshmipat University Jaipur

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination, December 2022

B.Tech, Semester-VII

Roll No.....

Course Code : CS2206

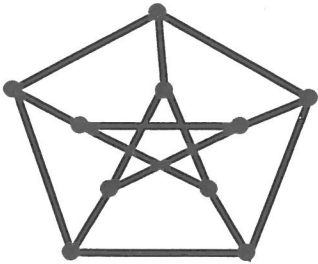
Time: 2 hours

Max. Marks: 30

Course Name: Design Automation for VLSI

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.

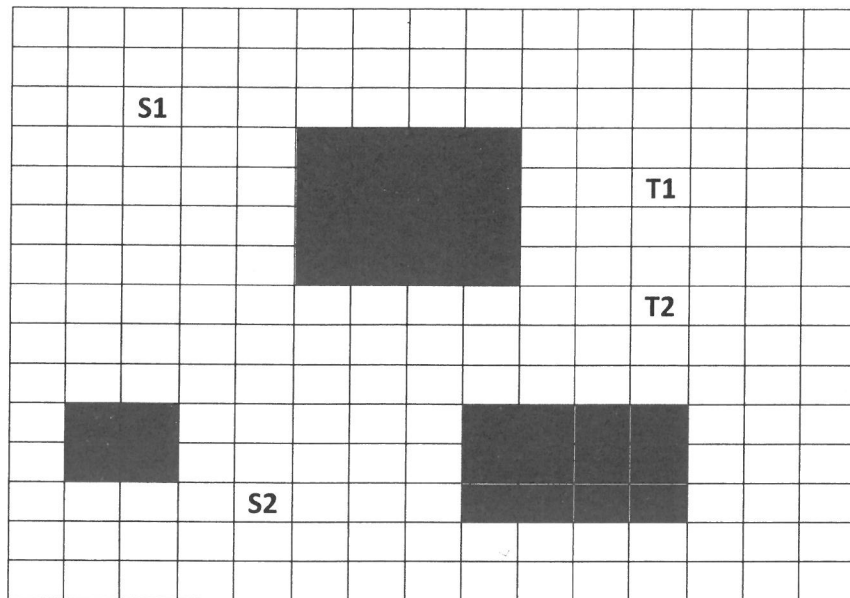
Q 1	A. What is the purpose of LVS in post layout verification? B. "Formal verification ensures that the design implementation satisfies the requirements of its specifications" – Justify. C. Using the design sequence of Standard cell-based design show that standard cell based design is simpler, manageable and systematic in comparison to full custom design of ASIC	02 03 03 CO 1 CO 2
Q2	A. If G is a connected plane graph with p vertices, q edges, and r regions, then prove that $p - q + r = 2$. B. State Kuratowski's theorem and using it - check the planarity of the following graph.  C. Using Kernighan-Lin algorithm for partitioning obtain the best possible partition for the following circuit graph	02 03 03 CO 2 CO 3

Q.4

- A. Differentiate between Floor planning, Placement and Chip planning in relation to ASIC design.
- B. Using Hadlock's Algorithm find the shortest path in the following grid for each of The two nets (showing clearly the steps)

03

03



- D. State why Grid based routing algorithms are found to be more advantageous as compared to Line-Probe algorithms.(mention time and space complexity)

02

CO1

CO2

CO3