

JK Lakshmipat University Jaipur
INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), February 2022
BTech, Semester I

Roll No.....

ES1111: Fundamentals of Automation Engineering I

Time: 2 hours

Max. Marks: 30

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Programmable Calculator is not allowed.

Q.1A Suppose we have to design a logic circuit to determine the best time to plant a garden. We consider three factors (inputs): 2.5

- Time, where 0 represents day and 1 represents evening;
- Moon phase, where 0 represents not full and 1 represents full;
- Temperature, where 0 represents 40°C and below, and 1 represents over 40°C.

We determine that the best time to plant a garden is **during the evening with a full moon.**

Design the truth table, draw the expression and implement using NOR gate only.

Q.1B Implement the following expression using 2 input NAND gate only

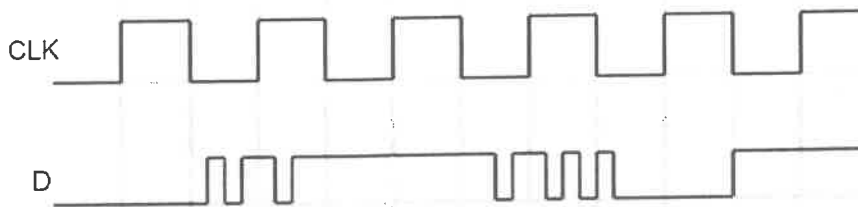
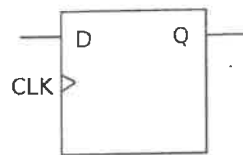
$$F = w(x + y - z) + xyz$$

Q.2 Design a combinational circuit to check for even parity of four bits. Draw the truth table for the parity generator. Draw the logic circuit diagrams for both the parity generator and parity checker. 05

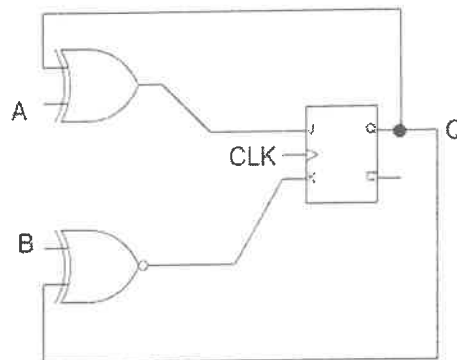
Q.3 A 4x1 multiplexer is to be used for implementation of function $F = \sum(0,1,3,5,7)$. 05
The truth table of the multiplexer is given in Table , S1 and S0 are the select lines and I0 to I3 are input lines. Show the implementation table and logical circuit diagram for implementation.

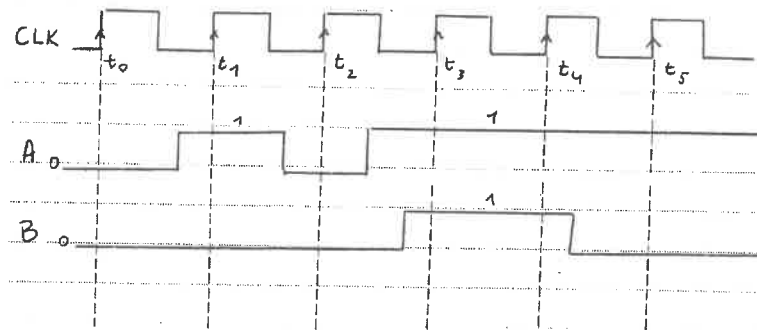
S1	S0	Y
1	1	I3
0	1	I2
1	0	I1
0	0	I0

- Q.4 Consider the following D type flip flop. Draw the timing diagram for output Q , assuming initial state $Q(0) = 0$. 05



- Q.5 Consider the following sequential circuit. Draw the timing diagram for output Q , assuming initial state $Q(0) = 0$. 05





- Q.6 A Low Pass Filter circuit consisting of a resistor of $1\text{K}\Omega$ in series with a capacitor of 10 nF is connected across a 1V sinusoidal supply. Calculate the cutoff frequency. What will be the output voltage at a frequency 10 times the cutoff frequency? Sketch the asymptotic approximation of transfer function magnitude. What is the value of cutoff frequency? 05

