

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular), November-December 2015

B. Tech in Electronics & Communication Engineering, Semester VII

Roll No.....

ECE728: VLSI DESIGN

Time: 3 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.

Q.1A	Very short answer type questions (10 questions @ 1 mark)	10
i.	Give the advantages of CMOS IC?	
ii.	What is Latch-up?	
iii.	What is Channel-length modulation?	
iv.	What will happen to the threshold of nMOS if Body terminal is connected to positive bias?	
v.	Define scaling.	
vi.	Draw the circuit of a CMOS inverter.	
vii.	What is defined within a port list?	
viii.	What are identifiers in VHDL?	
ix.	Define vector in VHDL.	
x.	What are the different types of modeling in VHDL?	

Q.2	Short answer type questions (4 questions @ 2.5 marks)	10
i.	Why N-mos transistor produces weak 1?	
ii.	What do you mean by $\beta_n = \beta_p$?	
iii.	Write about concept of regularity, modularity and locality in VLSI design.	
iv.	Differentiate between signal and variable assignment in VHDL.	

Q.3A	Compare Semi-custom and Full custom VLSI design style.	05
Q.3B	Why do we need isolation between MOS transistors fabricated on a single chip? Explain etched field-oxide isolation and LOCOS isolation technique in brief.	05

Q.4A	Discuss the effect of channel length modulation on drain current of NMOS transistor.	05
Q.4B	For two input XOR function, draw following implementations. (i) Full CMOS gate (ii) CMOS transmission gate(TG)	05

Q.5A	Design a CMOS logic gate for the function. $f = \overline{ab + ac + bd}$ using smallest number of transistors.	05
Q.5B	Specify the declaration form for package and package body with an example.	05
	OR	
Q.5B	Write a VHDL description for a SR latch.	
Q.6A	Draw the following circuit diagrams: (i) inverter with n-type MOS load (ii) two input NAND	05
Q.6B	Explain CMOS transmission gate in brief.	05
	OR	
Q.6B	Define or briefly discuss following: (i) Short channel effects (ii) Constant field scaling	
Q.7	Draw input and output waveforms during high to low transition of output for a CMOS inverter. Derive expression for τ_{PHL} .	10
	OR	
Q.7	Draw circuit of resistive load inverter. Derive V_{IH} , V_{IL} , V_{OL} and V_{OH} for resistive load inverter.	10
Q.8	Implement the following Boolean function using CMOS. $F = \overline{(C + D + E)} \cdot (B + A)$ Find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assume that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors.	10
	OR	
Q.8	Consider a MOS system with the following parameters: $t_{ox} = 200 \text{ \AA}$ $\phi_{GC} = 0.85 \text{ V}$ $N_A = 2 \times 10^{15} \text{ cm}^{-3}$ $Q_{ox} = q \times 2 \times 10^{11} \text{ C/cm}^2$ Determine the threshold voltage V_{TO} under zero bias at room temperature. Note that $\epsilon_{ox} = 3.97\epsilon_0$ and $\epsilon_{si} = 11.7\epsilon_0$.	
Q.9A	Write a VHDL code for function $Y = AB + \overline{CD}$ using (i) behavioral (ii) Structural modeling	10
Q.9B	(i) What is the main purpose of test bench? (ii) Write VHDL code for 2-to-4 decoder circuit.	10
	OR	
Q.9B	Derive the drain current equation for MOSFET using Gradual Channel Approximation.	10