

**JK Lakshmipat University Jaipur**  
**INSTITUTE OF ENGINEERING AND TECHNOLOGY**

End Term Examination (Regular), April 2018  
B. Tech. in Computer Science and Engineering, Semester IV

Roll No.....

CSE403: COMPUTER ARCHITECTURE AND ORGANIZATION

Time: 03 hours

Max. Marks: 100

---

**Instructions to students:**

1. Do not write anything other than your roll number on question paper.
  2. Assume suitable data wherever required and mention it clearly.
  3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
- 

**Q.1A Objective type multiple choice questions (10 questions @ 1 mark)**

10

- i. For inclusion to hold between two cache level L1 and L2 in a multilevel cache hierarchy, which of the following are necessary?
  1. L1 must be a write-through cache
  2. L2 must be write-through cache
  3. The associativity of L2 must be greater than that of L1
  4. The L2 cache must be at least as large as the L1 cache

A) 4 only                                      B). 1 and 2 only  
C) 1, 2 and 4 only                          D). 1, 2, 3 and 4
- ii. Generally Dynamic RAM is used as main memory in a computer system as it \_\_\_\_\_.

A). Consumes less power                      B). has higher speed  
C). has lower cell density                      D). needs refreshing circuitry
- iii. For a magnetic disk with concentric circular track, the latency is not linearly proportional to the seek distance due to  

A). Non-uniform distribution of requests  
B). Arm starting and stopping inertia  
C). Higher capacity of tracks on the periphery of the platter  
D). Use of unfair arm scheduling policies.
- iv. Which one of the following is the address generated by CPU?

A). Physical address                              B). Absolute address  
C). Logical address                                D). None of the mentioned
- v. In Reverse Polish notation, expression  $A*B+C*D$  is written as  

A).  $AB*CD*+$                                       C).  $A*BCD*+$

B).  $AB*CD+*$

D).  $A*B*CD+$

vi. Memory unit accessed by content is called \_\_\_\_\_.

A). Read only memory

B). Programmable Memory

C). Virtual Memory

D). Associative Memory

vii. Fragmentation is -

A). Dividing the secondary memory into equal sized fragments

B). Fragments of memory words used in a page

C). Dividing the main memory into equal size fragments

D). Fragments of memory words unused in a page

viii. Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called

A). Fragmentation

B). Paging

C). Mapping

D). None of the mentioned

ix. Which of the following requires a device driver?

A). Register

B). Cache

C). Main memory

D). Disk

x. The LRU provides very bad performance when it comes to \_\_\_\_\_

A). Blocks being accessed is sequential

B). When the blocks are randomized

C). When the consecutive blocks accessed are in the extremes

D). None of the mentioned

Q.2 Short answer type questions (4 questions @ 2.5 marks)

10

i. What is a port? Differentiate between serial and parallel port?

ii. Differentiate RISC and CISC architectures?

iii. What is meant by flash memory?

iv. What is the difference between a dependency and hazard?

Q.3A A non-pipelined processor has a clock rate of 2.5 GHz. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, the clock rate of the new processor has to be reduced to 2 GHz. What is the speedup achieved for a sequence of 100 instructions?

05

Q.3B What are the differences between Static Memory and Dynamic Memory?

05

Q.4A Identify all data dependencies in the following code; assuming that we are using the 5-stage MIPS pipelined data path. Which dependencies can be resolved via forwarding?

05

ADD R2,R5,R4

ADD R4,R2,R5

SW R5,100(R2)

ADD R3,R2,R4

- Q.4B What Are The Advantages Of Raid? What's The Difference Between Raid1 And Raid5? 05
- Q.5A A demand paging system with 4 page frames for page replacement. Give a diagram of all pages in memory after each page fault, for the following reference string: 05  
 2, 4, 5, 4, 5, 9, 2, 7, 4, 8, 9, 1, 6, 2, 2, 5, 3, 8  
 Compare the number of page faults for LRU, FIFO and Optimal page replacement algorithm
- Q.5B What is the purpose of System Bus? What are the three components in the system bus model of a digital computer? 05
- OR
- Q.5B Using a Stack organized computer with zero address operation instruction write a program to evaluate the arithmetic statement 05  

$$F = [(P + Q) / (R * S * T) - H] / (U * V + W - G)$$
 I). Using a general register computer with three-address instructions.  
 II). Using an accumulator type computer with one-address instructions.  
 III). Using a stack organized computer with zero-address instructions.
- Q.6A Consider you have 16384 x 8 RAM chips to build a main memory bank. 05  
 I). How many of these chips are needed to provide a memory capacity of 256 MB?  
 II). How many lines of the address bus must be used to access 1 GB of memory (one byte at a time)? How many of these lines will be common to all the chips?  
 III). How many lines must be decoded in order to select the right chip (activate chip select)?
- Q.6B Suppose a disk drive has the following characteristics: 05  
 • 5 surfaces  
 • 1024 tracks per surface  
 • 256 sectors per track  
 • 512 bytes/sector  
 • Track-to-track seek time of 8 milliseconds  
 • Rotational speed of 7500 RPM.  
 I. What is the capacity of the drive?  
 II. What is the access time?
- Q.7A Compare the speed, size, working principle and cost of different types of memories? 05

- Q.7B Write Short notes on 05
- I). EEPROM
  - II). Magnetic Disc
  - III). Blue Ray Disc

OR

- Q.7B What are the steps required for data transfer using DMA controller? When a DMA module take control of bus and while it remains control of bus, what does the processor do? 05

- Q.8A Why do we need I/O interface? How does I/O Bus communicate to I/O devices? What are the different ways in which computer buses can be used to communicate with memory and I/O? 10

- Q.8B Perform the indicated base conversion- 05
- a)  $(54)_8$  to base 5
  - b)  $(312)_4$  to base 7
  - c)  $(520)_6$  to base 9

OR

- Q.8B What are various modes of data transfer between the processor/Memory and I/O devices in a computer system? 05

- Q.9A Show how 32-bit addresses are divided into tag, index, and offset given the following cache descriptions: 10

- I). 32KB, byte addressable, 8-way set associative cache with 4 byte blocks.
- II). 16KB, byte addressable, direct mapped cache with 8 byte blocks
- III). 64KB fully associative cache with 64 byte blocks
- IV). Calculate the overhead for each of the above caches

- Q.9B What are different types of bus interfaces? Explain in detail USB bus organization. 05

OR

- Q.9B What is parallel processing and what are the different levels of parallel processing? How parallelism can be achieved in uni-processor system? 05