

JK LAKSHMIPAT UNIVERSITY, JAIPUR

INSTITUTE OF ENGINEERING AND TECHNOLOGY

End Term Examination (Regular/ Backlog), Apr-May. 2016

B. Tech. in Electronics & Communication Engineering, Semester IV

Roll No.....

ECE402: DIGITAL ELECTRONICS

Time: 3.0 hours

Max. Marks: 100

Instructions to students:

1. Do not write anything other than your roll number on question paper.
2. Assume suitable data wherever required and mention it clearly.
3. Writing appropriate units, nomenclature, and drawing neat sketches/schematics/ flow chart wherever, required are an integral part of the answer.
4. Use of Non-Programmable calculator is allowed.

Q.1A Objective type multiple choice questions (10 questions @ 1 mark) 10

- i. What do you understand with ASCII?
- ii. Convert the binary number 1001.0010_2 to decimal.
- iii. The programming technologies that are used in CPLD devices are all nonvolatile. (True/False)
- iv. What do you understand with FPGA?
- v. For designing 32×4 ROM, the size of decoder is
- vi. What do understand with EPROM?
- vii. Find out the value of k for converting 4 bit BCD code into Hamming code.
- viii. $A+AB+ABC+ABCD+\dots =$
- ix. In sign magnitude form of representation of a binary number, the MSB gives the
 - A. Length of the binary number
 - B. The base of the number system
 - C. The sign of the number system
 - D. None of the above
- x. What will be the range of signed decimal numbers that can be represented by 6-bits 1's complement number?

Q.2 Each Question is of 2.5 marks 10

- i. What do you understand with Hazards?
- ii. If 10 MHz square wave clock is applied in 5 bit ripple counter then determine the frequency of 3rd flip flop output.
- iii. What are the advantages of static RAM compared to Dynamic RAM?
- iv. A number of 512×8 bit memory chips are available. To design a memory organization of $3K \times 8$ memory. Identify the requirements of 512×8 memory chips and explain the details.

Q.3A A safe has 5 locks v, w, x, y and z; all of which must be unlocked for the safe to 05
open. The keys to the locks are distributed among five executives in the
following manner.





- Mr. P has keys for locks v and x.
- Mr. Q has keys for locks v and y.
- Mr. R has keys for locks w and y.
- Mr. S has keys for locks x and z.
- Mr. T has keys for locks v and z.

Find the minimum number of executives required to open the safe. Also implement it using NOR gates Only.

Q.3B Design a combinational circuit using a ROM. The circuit accepts a four bit 05
number and outputs a binary number equal to the half of the input number if
input number is even ('0' is not an even number) otherwise gives zero as output.
Also write the ROM dimensions.

Q.4A i. What will be the 8 bit 2's complement representation of decimal number 05
(-44).
ii. Assume the number $(10011001)_2$ in 2's complement representation. What
will be the decimal equivalent of the number?

Q.4B Simplify the following Boolean expression using K-map and implement the 05
result with NOR gate only

$$F(A,B,C,D) = A'B'C' + AC'D' + AB' + ABCD' + A'BC$$

Q.5A Design a mod 7 asynchronous up counter using JK flip flops. Write the state 05
diagram and the timing diagram for the same. The counter counts during the
+ive edge of the clock.

Q.5B Consider the following four codes 05

Code A	Code B	Code C	Code D
0001	000	01011	000000
0010	001	01100	001111
0100	011	10010	110011
1000	010	10101	

Which of the following properties are satisfied by each of the above codes?

- a. Detects single error
- b. Detects double error
- c. Corrects single errors
- d. Corrects double errors
- e. Corrects single error and detects single error

Q.6A What is the race around condition in JK Flip Flop? What are the different 05
methods to overcome this problem? Explain Master-Slave method in detail.

Q.6B A 4 bit number is represented by ABCD with D as LSB. Design a logic circuit 05
that will produce a 1 whenever the input is greater than 0010 but less than 1000.

Use minimum number of NAND gates.

OR

Q.6B Implement the following equations using a suitable PLA circuit.

05

$$A(x,y,z) = \sum m(1,2,3,4)$$

$$B(x,y,z) = \sum m(0,1,3,6,7)$$

Q.7A Implement the following equations using a suitable PAL circuit.

07

$$A(x,y,z) = \sum m(1,2,4,6)$$

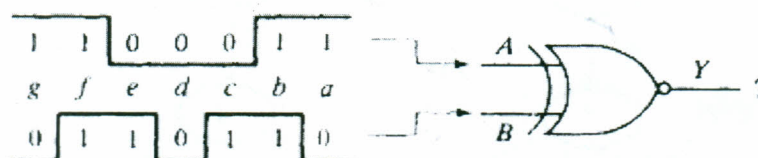
$$B(x,y,z) = \sum m(0,1,3,6,7)$$

$$C(x,y,z) = \sum m(1,2,4,6,7)$$

$$D(x,y,z) = \sum m(1,2,3,5,7)$$

Q.7B What will the pulse train at the output of the XNOR gate shown in given Fig.?

03



Q.8 A sequential circuit has two flip flops (A and B), two input x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y'$$

$$K_A = B'xy'$$

$$J_B = A'x$$

$$K_B = A + xy'$$

$$z = Axy + Bx'y'$$

- Draw the logic diagram the circuit.
- Tabulate the state table.
- Derive the state equation for A and B.

OR

Q.8 Draw the ASM chart and state diagram for synchronous circuit having the following descriptions. The circuit has control input C, clock and output a, b and c.

- If $C=1$, on every positive edge, the output changes in the sequence. $000 \rightarrow 001 \rightarrow 011 \rightarrow 111 \rightarrow 000$ and repeats
- If $C=0$, the circuit holds in the previous state.

Q.9A We can expand the word size of a RAM by combining two or more RAM chips.

05

For instance, we can use two 32×8 memory chips where the number 32 represents the number of words and 8 represents the number of bits per word. To obtain a 32×16 RAM, the number of words remains the same but the length of each word will two bytes long. Draw a block diagram to show how We can use two 16×4 memory chips to obtain a 16×8 RAM.



OR

Q.9A Implement the following expression using a single 8:1 Multiplexer.

05

i. $Y(A,B,C) = \sum m(0,1,2,6,7)$

ii. $Y(A,B,C) = \prod M(0,1,4,5)$

Q.9B For the given state diagram,

2+5+8

i. Draw State Table

=15

ii. Draw reduced State table and diagram

iii. Design the circuit using D Flip Flop for next state and output.

