

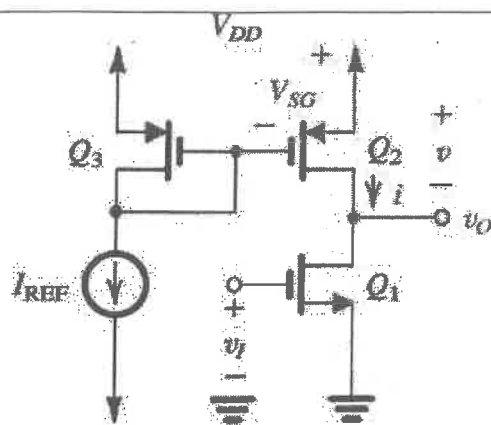
JK LAKSHMIPAT UNIVERSITY JAIPUR
INSTITUTE OF ENGINEERING AND TECHNOLOGY
End-Term Examination

Programme: B.Tech
Course Name: Analog Electronics
Maximum Marks: 30

Semester: 4th
Course Code: EE1124
Time Allowed: 2:30 Hours

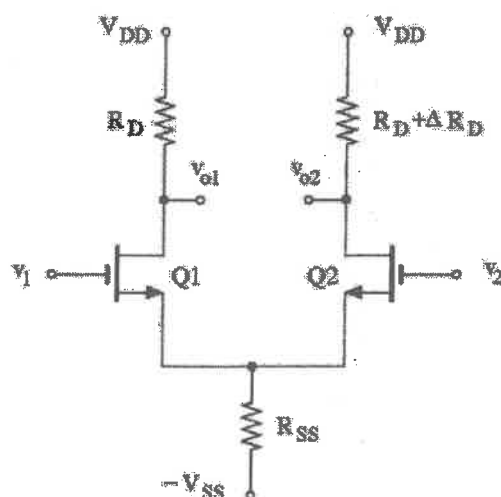
- Do not write anything other than your roll number on question paper.
- Mention all the assumptions for your answers clearly.
- The student, before starting to write the solutions, should please check the question paper for any discrepancy and ensure that they have been delivered the question paper of right course code.
- Total 5 Questions are there.
- * *Calculator allowed.*

No.		Question	Marks	CO
1.		Design the single-stage CMOS amplifier with current mirror load for a gain of 20 V/V at a power consumption of 1 mW. Assume that the input common mode voltage level is 1 V, and the input-pair transistors operate at the edge of saturation. Given $V_{DD}=1.8\text{ V}$, $V_{THn}=0.5\text{ V}$, $V_{THp}=-0.4\text{ V}$, $\mu_n C_{ox}=100\text{ }\mu\text{A/V}^2=2\mu_p C_{ox}$, and $\lambda_n=0.1\text{ V}^{-1}=0.5\lambda_p$. Also draw the schematic of the circuit.	5	4
2	a	Explain with operation and behaviour of an P channel MOSFET with help of labelled schematic diagram and output I-V characteristics.	3	1
	b	A CMOS inverter is operating at a supply voltage $V_{DD}=1.8\text{ V}$ and driving a capacitive load $C_L=10\text{ pF}$. The inverter switches at a frequency of $f=100\text{ MHz}$ with a 50% duty cycle square wave input. (a) Derive the expression for dynamic power consumption of the CMOS inverter and compute its value. (b) If the inverter has a leakage current of 1 nA when idle, calculate the static power consumption. (c) Determine the total average power consumption.	3	
3	a	Design and Explain functioning of a Cascode current mirror. OR Design and Explain the functioning of Wide swing current Mirror.	4	2
	b	1) A CMOS 1:1 current mirror circuit is shown $V_{DD}=3\text{ V}$, $V_{tn}= V_{tp} =0.6\text{ V}$, $K_n'=200\text{ }\mu\text{A/V}^2$, $K_p'=65\text{ }\mu\text{A/V}^2$, $L=0.4\text{ }\mu\text{m}$, $W=4\text{ }\mu\text{m}$, $V_{Dn}=20\text{ V}$, $ V_{Dp} =10\text{ V}$, $I_{REF}=100\text{ }\mu\text{A}$. What is the small-signal voltage gain, A_v ?		



Or

2. Find CMRR. (Q1 and Q2 are identical and ignore r_o)



4. Design a Common source (CS) amplifier with a low frequency small signal voltage gain of 17dB. For transistor use $V_t = -0.42\text{V}$, $\mu_p C_{ox} = 45\mu\text{A/V}^2$ and $\lambda = 0$. Use channel Length = $2\mu\text{m}$. $V_{DD} = 1.8\text{V}$, and you should design for output voltage = $V_{DD}/2$ and bias transistor current of $100\mu\text{A}$.

5. A CMOS inverter with minimum sized transistors has $\beta_n = 0.2\text{mA/V}^2$, $\beta_p = 0.1\text{mA/V}^2$ and $V_{tn} = |V_{tp}| = 0.6\text{V}$. Assume $V_{DD} = 3.3\text{V}$.

a) What is the inverter gate switching threshold (midpoint) voltage V_M ?

b) What is the resistance for each transistors using our general expression for MOSFET resistance in saturation?

c) What are the rise and fall times of this circuit if the parasitic capacitance at the output is 9fF ?

d) If a load capacitance, $C_L = 25\text{fF}$ is added to the output, what are the new rise and fall times?

e) What are the propagation delays (Rise and Fall) for this circuit considering both parasitic and load capacitances?

f) What is the Total propagation delay of the circuit considering both parasitic and load capacitances?