



A Compact Floating-Gate Diode-Connected MOSFET Memristor Emulator for Low-Voltage Analog Applications

Kunal Kaushik¹ · Mukul Jangid¹ · Gaurav M. Khanal² · Aaishi Dubey¹ · Sanjeev Kumar³ · Satinder K. Sharma⁴ · Arun K. Singh¹ 

Received: 4 August 2025 / Revised: 5 November 2025 / Accepted: 7 November 2025

© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2025

Abstract

This research presents a miniature charge-controlled memristor emulator that employs a single MOSFET and a single MOSCAP, operating without supplementary bias. The design supports a wide frequency range from 1 kHz to 40 MHz at different capacitance and functions at a low supply voltage of ± 0.45 V. The emulator, developed and validated in Cadence Virtuoso using standard 90 nm GPDK CMOS technology, exhibits notable memristive behavior defined by a pinched hysteresis loop in the I - V plane. Its streamlined architecture reduces component count and power consumption compared to conventional systems. The proposed emulator is evaluated in two application domains. Initially, it is included into a CMOS Schmitt trigger, demonstrating configurable threshold levels and programmable hysteresis, so enhancing noise immunity. Secondly, it is employed in memristor-capacitor-based filters (low-pass, high-pass, and band-pass), exhibiting frequency-dependent performance and accurate tuning via memristance modulation. The simulation results validate its dynamic switching, stability, and performance across the whole operational frequency spectrum. The design offers a practical, scalable, and energy-efficient solution for analog computing, neuromorphic systems, and reconfigurable signal processing.

Keywords Memristor emulator · MOSFET · MOSCAP · Charge-controlled · Wide frequency range · GDPK

1 Introduction

Since Leon Chua's 1971 [1] suggestion of the memristor as the elusive 4th fundamental circuit element linking charge and flux [2], memristive devices have attracted considerable interest for non-volatile memory, neuromorphic computing, adaptive

Extended author information available on the last page of the article

analog electronics, and chaotic signal generation [3]. The memristor is the fourth fundamental component [4], distinguished by its reliance on the historical flow that currently passes through it [5]. The first memristor was created in HP laboratories using titanium dioxide (TiO_2), which features a switching layer that defines two resistive states: high resistance (R_{off}) and low resistance (R_{on}) [6].

The external voltage regulates the transition between resistance states. For simulation purposes, researchers utilized various methodologies, including SPICE modeling, including both physics-based and behavioral memristor models [7–11]. Authentic physical memristors—generally employing metal oxide resistive switching or phase change materials—demonstrate promising performance but are limited by device variability, durability constraints, and integration challenges with traditional CMOS technology. Researchers endeavor to recreate memristor functioning using analog components that include both active and passive elements. The analog building blocks comprise operational transconductance amplifiers (OTA) [12–15], current conveyor-II (CCII) [16–18], voltage differencing current conveyors (VDCC) [19–21], differential voltage transconductance amplifiers (VDTA) [22–24], and current feedback operational amplifiers (CFOA) [25], among others. Researchers aim to streamline memristor emulator circuits by reducing the number of components needed, thereby decreasing design complexity and enhancing performance, in light of the substantial size and extensive component requirements of conventional systems. Memristor emulators were developed using diodes [26, 27], MOS transistors [28–33], and BJTs [34]. These types of memristor emulators are less sophisticated and more easily integrated into existing CMOS-based designs. Recently, CMOS-based memristor emulators have emerged as a robust platform for prototyping memristive behavior; they replicate the characteristic pinched hysteresis I–V curve and state-dependent resistance using established silicon technology, allowing designers to investigate circuit and system-level applications such as Schmitt triggers, analog filters, chaotic circuits, digital logic gates, integrators/differentiators, and neuromorphic computing.

We present a straightforward, fundamental memristor emulator configuration including exclusively one n-channel MOSFET and one MOS capacitor (MOSCAP) built using 90 nm CMOS technology. The circuit demonstrates memristive behavior, characterized by pinched hysteresis and loop area modulation in relation to frequency, by employing the MOSCAP as an on-chip charge storage element and the voltage-controlled conductance of the MOSFET, all without the need for external resistors or bias currents. This Memristor emulator can be employed to create advanced memristor-CMOS or just memristor-based analog and digital circuits. This work delineates the design and validation of a Schmitt trigger and analog filters predicated on a memristor emulator, employing simulation results. Section 2 describes the circuit topology and operating principles of the single-MOSFET/MOSCAP emulator. Section 3 presents detailed simulation results, including frequency sweeps, Capacitance variability, variation in temperature and Series/Parallel topology. Section 4 discusses analog applications. Finally, Section 5 concludes comparison table and outlines future directions, such as multi-element networks for neuromorphic reservoirs and on-chip learning applications. By demonstrating that a MOSFET plus MOSCAP suffices to replicate ideal memristive behavior at kilohertz frequencies and sub-volt

supplies, this work opens a pathway toward ultra-compact, low-power memristor-inspired circuits fully compatible with standard CMOS workflows.

2 Proposed Memristor Emulator

2.1 Overview and Circuit Description

A minimal-component memristor emulator is proposed, employing a solitary NMOS transistor and a gate-connected MOS capacitor (MOSCAP), as depicted in Fig. 1. The architecture eliminates the need for external biasing circuitry, enabling operation at an ultra-low voltage of ± 0.45 V. The core principle involves the modulation of the gate voltage exclusively through the temporal accumulation of charge. The accumulated charge on the gate-connected MOSCAP dynamically alters the NMOS gate-to-source voltage, thus affecting the channel resistance. The system retains a record of prior current flow via gate charge, so simulating a charge-controlled memristive device. The circuit is fabricated using conventional 90 nm GPDK CMOS technology and verified in Cadence Virtuoso.

In contrast to several current implementations that function in the triode area or necessitate active biasing circuits [25, 26], the suggested design keeps the NMOS

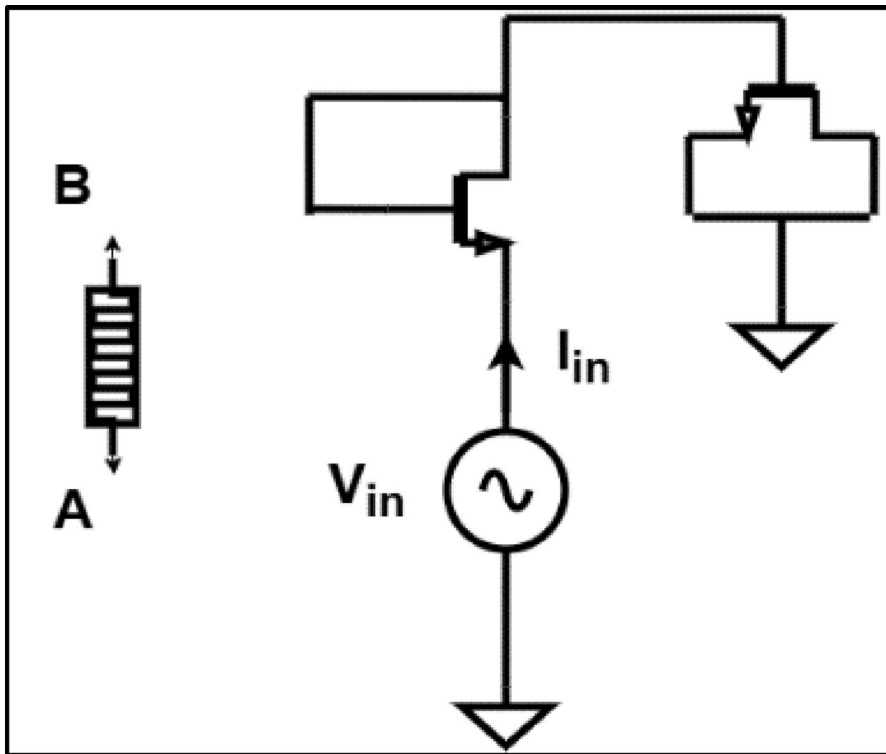


Fig. 1 Proposed emulator circuit

transistor solely in the saturation region, facilitating improved control of nonlinearity and heightened sensitivity to variations in gate voltage. This architecture facilitates operation over an extensive frequency range (500 Hz to 40 MHz) and provides compatibility with analog signal processing functions, including filtering and threshold-based switching.

2.2 Mathematical Modeling of proposed memristor emulator

A diode-connected NMOS operates in the saturation region due to $V_{DS} = V_{GS}$, which inherently satisfies $V_{DS} \geq V_{GS} - V_T$ for $V_T > 0$ V. To demonstrate that the circuit behaves as a memristor emulator, we begin with the current expression for an NMOS operating in the saturation region:

$$I_D = I(t) = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS}(t) - V_{Th})^2 \quad (1)$$

where $V_{GS}(t) = V_G(t) - V_{in}(t)$

$$I_D = I(t) = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_G(t) - V_{in}(t) - V_{Th})^2 \quad (2)$$

here $I(t)$ is the drain current, μ_n represents the carrier mobility, C_{ox} is the gate oxide capacitance per unit area. The aspect ratio of the NMOS transistor is given by $\frac{W}{L}$. $V_G(t)$ and V_{Th} represent the gate voltage and threshold voltage.

The gate voltage $V_G(t)$ is determined by the charge accumulated on the MOS capacitor:

$$q(t) = C_{ox} V_G(t) \Rightarrow V_G(t) = \frac{q(t)}{C_{ox}}$$

Substituting $V_G(t)$ into the current equation yields:

$$I_D(t) = I(t) = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(\frac{q(t)}{C_{ox}} - V_{in}(t) - V_{Th} \right)^2$$

This expression shows that the current is solely a function of $Q(t)$, the integral of the past input current:

$$q(t) = \int I_{in}(t) dt \Rightarrow q'(t) = I_{in}(t).$$

Let $\beta = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$, $X(t) = \frac{q(t)}{C_{ox}} - V_{in}(t) - V_{Th}$.
 $I_{in}(t) = \beta [X(t)]^2$

$$\sqrt{I_{in}(t)} = \sqrt{\beta} [X(t)] = \sqrt{\beta} \left(\frac{q(t)}{C_{ox}} - V_{in}(t) - V_{Th} \right) \quad (3)$$

$$V_{in}(t) = \frac{q(t)}{C_{ox}} + V_{th} + \frac{1}{\sqrt{\beta}} \sqrt{I_{in}(t)} \quad (4)$$

Equation (4) is exact, provided that $\frac{q(t)}{C_{ox}} \geq V_{th}$ (so that $X(t) \geq 0$).

A charge-controlled memristor [35] is defined by:

$$\begin{cases} V_{in}(t) = M(q(t)) \cdot I_{in}(t) \\ q'(t) = I_{in}(t) \end{cases} \quad (5)$$

where $M(q(t))$ is a function only of the total stored charge $q(t)$. We already have $q'(t) = I_{in}(t)$ from (1). To match the first equation of (5), we need to rewrite (4) in the form $V_{in}(t) = M(q(t)) \cdot I_{in}(t)$

$$V_{in}(t) = \frac{q(t)}{C_{ox}} + V_{th} + \frac{1}{\sqrt{\beta}} \sqrt{I_{in}(t)}$$

Divide both sides by $I_{in}(t)$:

$$M\left(q(t), I_{in}(t)\right) = \frac{V_{in}(t)}{I_{in}(t)} = \frac{\frac{q(t)}{C_{ox}} + V_{th}}{I_{in}(t)} + \frac{1}{\sqrt{\beta}} \frac{1}{\sqrt{I_{in}(t)}} \quad (6)$$

In other words, the NMOS+MOSCAP pair in true saturation does not yield a purely charge-controlled memristor law of the form $V_{in}(t) = M(q(t)) \cdot I_{in}(t)$. So that is

$I_{in}(t)$ much smaller than $\frac{q(t)}{C_{ox}} + V_{th}$ from Eq. 6

Concretely, if

$$\sqrt{I_{in}(t)} \ll \frac{q(t)}{C_{ox}} + V_{th}.$$

then the term $\frac{1}{\sqrt{\beta}} \frac{1}{\sqrt{I_{in}(t)}}$ (the second term in Eq. (6)) becomes negligible com-

pared to $\frac{q(t)}{C_{ox}} + V_{th}$. Under this “small-current” approximation, we may drop the $\frac{1}{\sqrt{I_{in}(t)}}$ portion and write

$$M\left(q(t), I_{in}(t)\right) \approx \frac{V_{in}(t)}{I_{in}(t)} = \frac{q(t)}{C_{ox}} + V_{th}, \quad (7)$$

The emulator’s instantaneous resistance effectively depends only on $q(t)$. Consequently, this single-NMOS/MOSCAP pair emulates a charge-controlled memristor over 500 Hz–40 MHz at ± 0.45 V, with negligible standing current in the MOSCAP and designed has been verified in 90 nm cmos pdk in cadence virtuoso. Finally, when a sinusoidal input $V_{in}(t) = A \sin(\omega t)$ is applied at the source, Eq. (4) implies conduction begins only when $A \sin(\omega t) \geq \frac{q(t)}{C_{ox}} + V_{Th}$. Above this threshold,

$q' = \beta \left(A \sin(\omega t) - \frac{q(t)}{C_{ox}} - V_{Th} \right)^2$ drives q (and thus $M(q)$) upward until the sinusoid falls below the updated threshold, after which q is held constant. Over successive cycles, $M(q)$ therefore steps up whenever $A \sin(\omega t)$ crosses the rising threshold and remains “frozen” otherwise. This cycle-to-cycle dependence on the integral of I produces the characteristic pinched hysteresis in the I – V plane, confirming true memristive dynamics in the diode-connected NMOS emulator.

2.3 Practical Considerations and Characteristics

The employment of a MOSCAP as the charge storage element ensures reliable retention of the state variable ($q(t)$) even at low frequencies (down to 500 Hz). Consistently operating inside the saturation region enhances the nonlinearity and stability of the response, which is beneficial for emulating genuine memristive dynamics. The absence of resistive elements and active biasing significantly reduces area and power consumption.

Simulations performed in Cadence Virtuoso confirm suitable memristive behavior, including pinched hysteresis loops under sinusoidal excitation and dynamic resistance variations. The developed emulator has been successfully integrated into analog signal processing applications, such as Schmitt triggers and filter circuits (low-pass, high-pass, and band-pass), where the memristor affects system dynamics based on prior input history.

3 Simulations Results

The simulation findings were obtained using the Cadence Virtuoso tool with a 90 nm GPDK technology node and without external biasing. The initial validation of this memristor emulator model utilizes technology featuring a transistor aspect ratio (W/L) of 120/100 nm. The transient response of the proposed memristive device is measured by applying the sinusoidal voltage of 0.45 V at 5 kHz. The obtained results in Fig. 2a, b are compared with the theoretical values obtained by developing a Python-based mathematical model which demonstrates close agreement across all the cycles. The slight variations in simulation and theoretical results arise from non-ideal MOSFET behavior in the test structure i.e. channel-length modulation and series resistance produce an effective output conductance that alters loop slope, field-dependent mobility and velocity saturation reduce conduction on one polarity and skew the waveform, body-effect induced threshold shifts change the switching points for opposite lobes, and MOS-capacitor leakage and gate/subthreshold currents introduce asymmetry and baseline offset.

The capacitance-dependent I – V characterization is then performed at 1 kHz, 5 kHz, 20 kHz, 50 kHz, 100 kHz, 500 kHz, 1 MHz, 20 MHz and 40 MHz in Figs. 3 and 4 exhibiting the hysteresis curves. Within the examined parameter window, increasing the device capacitance produces a systematic enlargement of the hysteresis loop (increased loop area and opening) which is consistent with slower effective state dynamics and enhanced charge accumulation. These findings identify capacitance as

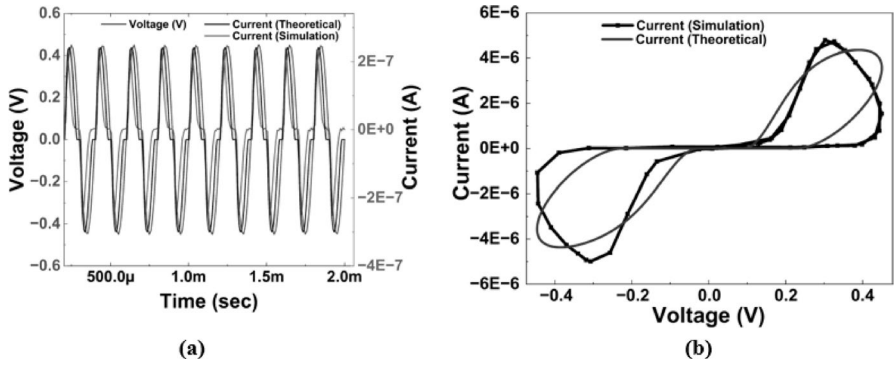


Fig. 2 Simulated and theoretical **a** Current and Voltage as function of time and **b** I - V Characteristics of proposed device exhibiting hysteresis

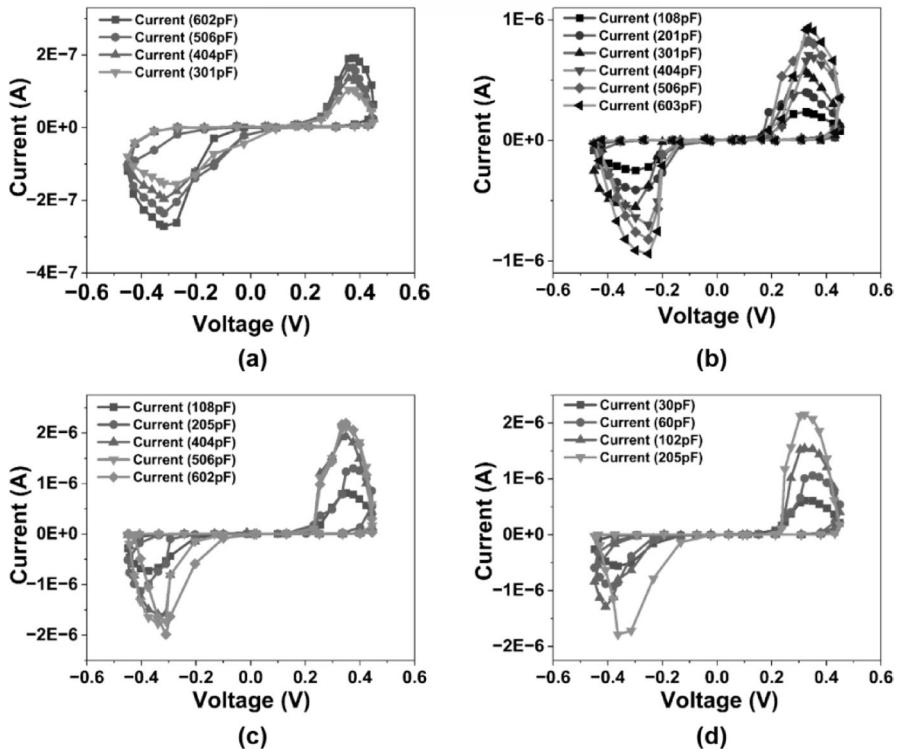


Fig. 3 I - V characteristics of the proposed emulator at different MOS capacitance at **a** 1 kHz, **b** 5 kHz, **c** 20 kHz, **d** 50 kHz

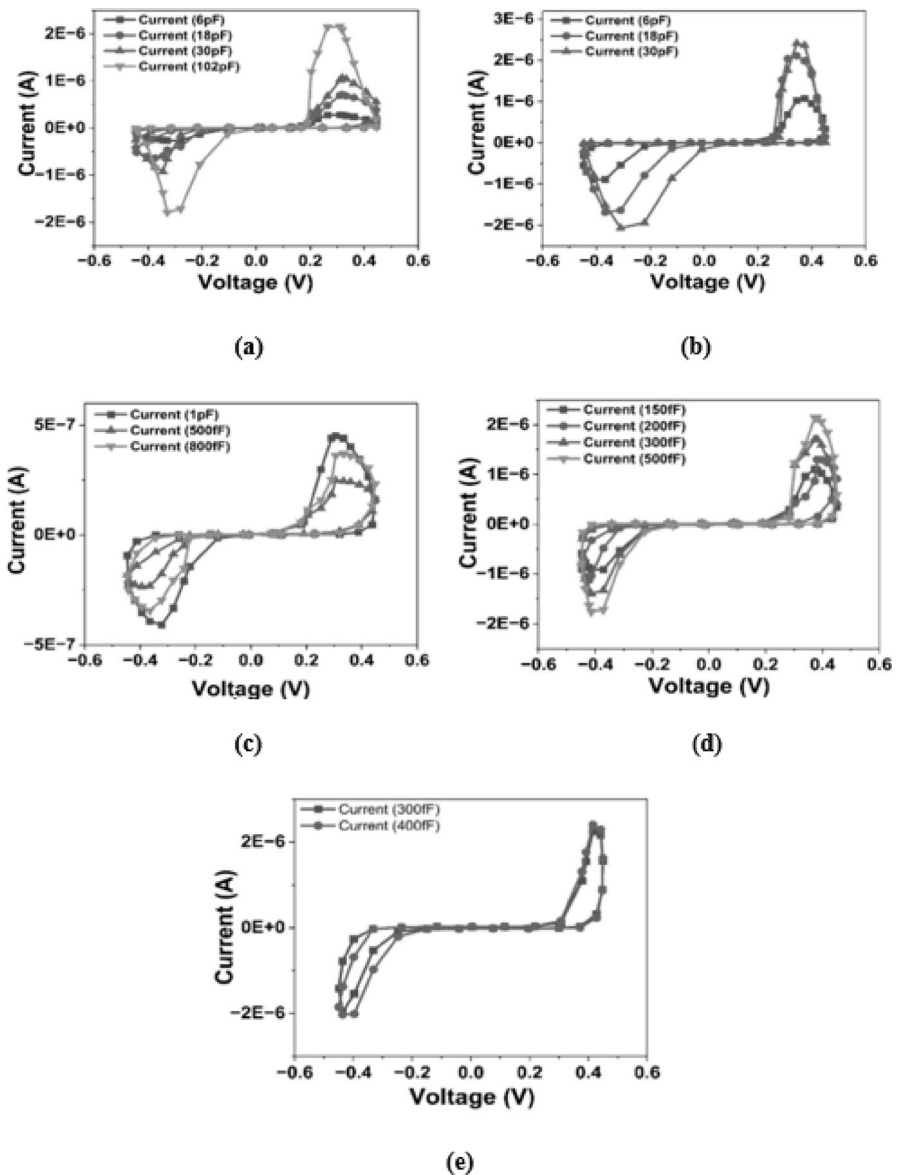


Fig. 4 I - V characteristics of the proposed emulator at different MOS capacitance with different frequency **a** 100 kHz, **b** 500 kHz, **c** 1 MHz, **d** 20 MHz, **e** 40 MHz

a controllable parameter for tuning the memristive hysteresis and switching behavior, with direct implications for memory retention and neuromorphic circuit design.

From Eq. 7, it is evident that memristance of the emulator depends the stored gate charge $q(t)$, which is varying for the applied sinusoidal signal $V_{in}(t) = A \sin(\omega t)$ as

$$\Delta q = \int_0^T I(t) dt \sim M(T) = M\left(\frac{1}{\omega}\right) \quad (8)$$

where $T = 2\pi/\omega$ represents the period.

In the developed model, the change in device resistance between high- and low-resistance $\Delta R = R_{\text{HRS}} - R_{\text{LRS}}$, is proportional to the state change Δq . Accordingly,

$$\Delta R \propto \Delta q \propto \frac{1}{\omega} \quad (9)$$

The small variation in ΔR results the change in high- and low-resistive states as $R_{\text{HRS}} = R_0 + 1/2\Delta R$ and $R_{\text{LRS}} = R_0 - 1/2\Delta R$ which in turn affects the memory-window ratio ($W = R_{\text{HRS}}/R_{\text{LRS}}$) in Eq.10

$$W = \frac{R_0 + 1/2\Delta R}{R_0 - 1/2\Delta R} \approx 1 + \frac{\Delta R}{R_0} \propto 1 + \frac{1}{\omega} \quad (10)$$

Here, $W \propto 1/\omega$ in the high-frequency regime and results $W \rightarrow 1$ at $\omega \rightarrow \infty$.

The I - V Characteristic of proposed emulator is shown at different frequencies for two capacitance values 102 pF and 500 fF in Fig. 5a, b, respectively. The obtained results demonstrates that for capacitance 102 pF, hysteresis loop is better for frequency variations from 5 to 100 kHz, however, for capacitance 500 fF better hysteresis loop are achieved from 1 to 40 MHz. Fig. 5c, d, show the HRS/LRS ratio, a measure of hysteresis loop, at capacitance of 102 pF and 500 fF, respectively. It is observed that HRS/LRS ratio tends to decrease to near unity at higher frequencies which suggests that hysteresis loop in I - V characteristics of emulator disappeared when frequency is increased beyond 40 MHz.

Figure 6 compares the memristor-emulator's I - V loops at 0 °C (black), 27 °C (red), and 60 °C (blue). As temperature rises from 0 to 27 °C, the conduction threshold shifts downward (≈ 0.35 V $\rightarrow$ 0.32 V) and peak current increases ($\approx 5 \times 10^{-7}$ A $\rightarrow$ 8×10^{-7} A), due to modest V_{th} reduction and limited mobility loss. At 60 °C, the threshold further falls to ≈ 0.30 V, but peak current drops to $\approx 6 \times 10^{-7}$ A because mobility degradation and higher MOSCAP leakage limit charge accumulation. Negative-cycle turn-off voltages and currents show similar trends. Overall, hysteresis area grows from 0 to 27 °C then contracts at 60 °C, reflecting the balance between threshold roll-off and leakage.

The red trace in Fig. 7c represents the emulator arranged in series in Fig. 7a, whereas the black trace depicts the parallel configuration in Fig. 7b. Both devices exhibit the distinctive “pinched” hysteresis loop of an ideal memristor, with current returning to zero at zero voltage. The parallel architecture offers an increased dynamic range and higher ON state current—approximately 1.2 μ A at +0.4 V—attributable to dual conduction pathways, while the series configuration shows a reduced current variation (≈ 0.6 μ A) but exhibits more abrupt state transitions near ± 0.3 V. In the Fig. 8a, b, the black trace shows a series of ten 0 $\rightarrow$ 0.45 V rectangular

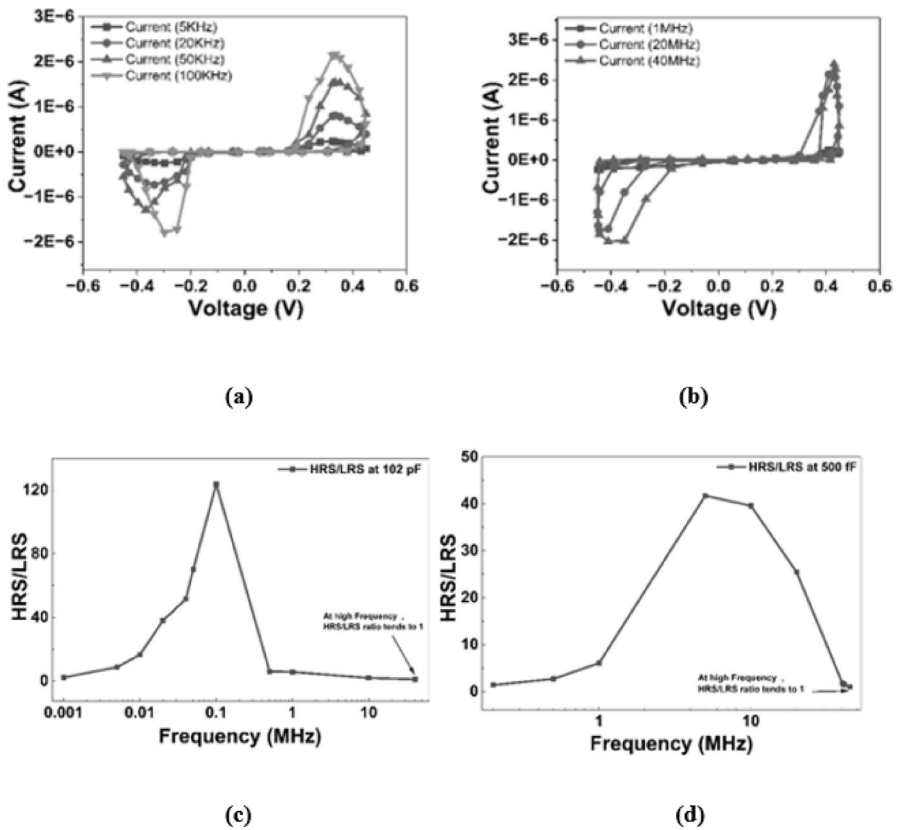


Fig. 5 I - V Characteristics are shown at different frequency with same capacitance value **a** MOS capacitance value = 102 pF, **b** MOS capacitance value = 500 fF, **c** HRS/LRS ratio at 102 pF, **d** HRS/LRS ratio at 500 fF

voltage pulses (100 μ s wide, 100 μ s off) over a 1 ms window, while the red trace shows the corresponding current response: an initial peak of $\approx 2.7 \times 10^{-8}$ A that steadily decreases with each pulse. On the right, the memristance (plotted in Fig. 8c) rises in a clear staircase fashion from about $1.5 \times 10^7 \Omega$ to $\approx 2.9 \times 10^7 \Omega$ across the ten pulses and remains essentially unchanged during the zero-voltage intervals. This progressive increase and stable retention of the high-resistance state between pulses conclusively demonstrates the emulator's programmability and non-volatility, key requirements for reliable analog memory and in-memory computing applications.

4 Analog Applications

Memristor emulators, distinguished by their inherent hysteresis and variable resistance capabilities, offer substantial potential for advancement in analog circuit design. By employing dynamic memristance modulation, these emulators offer reconfigurable and programmable functionalities in critical circuits such as Schmitt triggers,

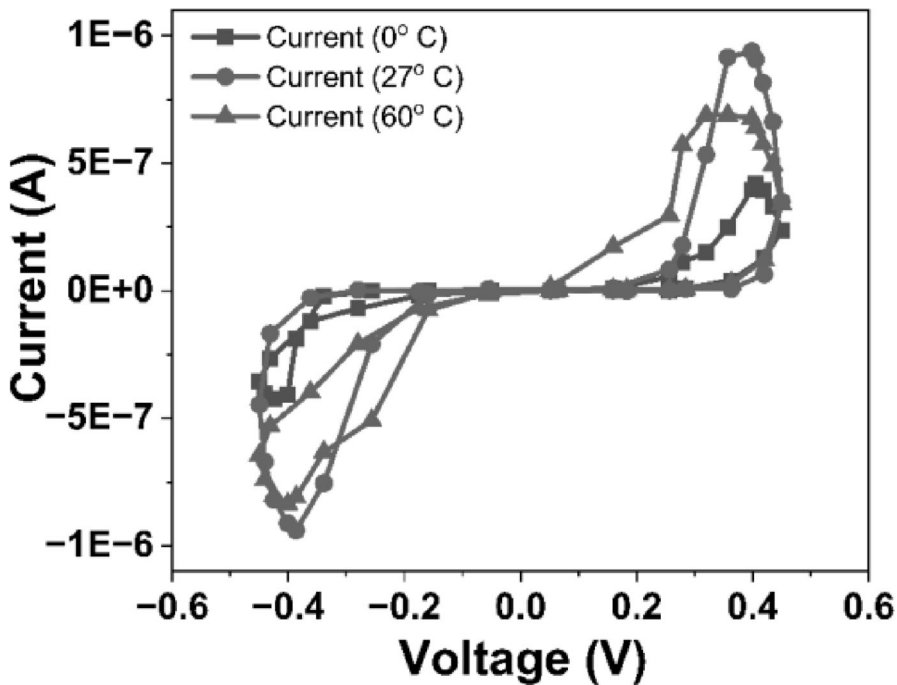


Fig. 6 Temperature variation of I - V characteristics at 5 kHz frequency and 301pF MOS Capacitance

filters, and oscillators. We analyse their application in Schmitt triggers, low-pass, bandpass, and high-pass filters, supported by theoretical frameworks and experimental validations.

4.1 Schmitt Trigger with Tunable Hysteresis

A Schmitt trigger is a critical circuit for noise immunity and waveform shaping, relying on its hysteresis window to stabilize switching thresholds. Integrating a memristor emulator into the Schmitt trigger replaces traditional resistors with a voltage-dependent memristance, enabling programmable hysteresis.

$$V_{TH} = V_{sat} \left(\frac{MR}{R} \right), V_{TL} = -V_{sat} \left(\frac{MR}{R} \right) \quad (11)$$

For instance, the transient analysis of an NMOS-based memristor emulator (Fig. 9) demonstrates a hysteresis window of ± 800 mV at 1 kHz, where the output toggles between ± 900 mV as the input crosses adaptive thresholds. The memristor's state-dependent resistance dynamically adjusts the trigger points based on the input history, enhancing robustness against signal jitter. This aligns with the floating memristor emulator design by Suresha et al. [28] which achieved Schmitt trigger operation with Type-II hysteresis, validated in amplitude demodulation circuits. Such configurability is pivotal for adaptive signal conditioning in low-power sensor interfaces.

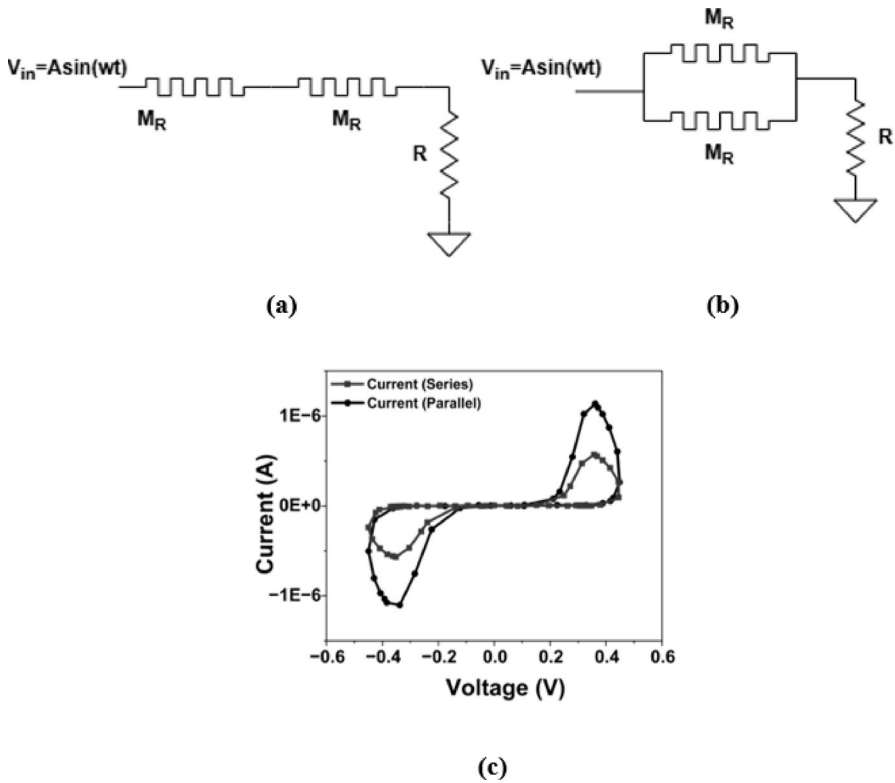


Fig. 7 Shows the quasi-DC I - V characteristics of the proposed memristor emulator under a bipolar voltage sweep (-0.6 V to $+0.6$ V) at $R = 1$ k ohm

4.2 Low-Pass Filter (LPF) and High-Pass Filter (HPF)

Figure 10a, b show the design of a typical high pass filter and low pass filter utilizing the proposed memristor emulator and a capacitor of 500 fF, respectively. Considering instantaneous resistance (M_R) of the proposed memristor emulator, both the circuits inherit the first-order transfer functions as $H(j\omega) = \frac{j\omega}{1+j\omega}$, and $H(j\omega) = \frac{1}{1+j\omega}$, for high-pass and low-pass filters, respectively, where $f_C = \frac{1}{2\pi}$ and $\tau = M_R C$. The instantaneous cut-off or -3 dB corner frequency for both the filters can be estimated as $f_c(t) = 1/(2\pi M(q(t))C)$. The M_R is state-dependent i.e. $M_R = M(q(t))$ (with $q'(t) = I_{in}(t)$), hence, the changes in memristance directly translate into shifting of the time constant (τ). Figure 10c, d show the output of high pass and low pass filter while applying AC amplitude of 1 V at different memristance states which are estimated from Fig. 8c. The memristance varies from 18 to 30 M Ω in time domain which gives the dynamic variation in cut off frequency (f_c), hence, filter's time constant as shown in Fig. 10e.

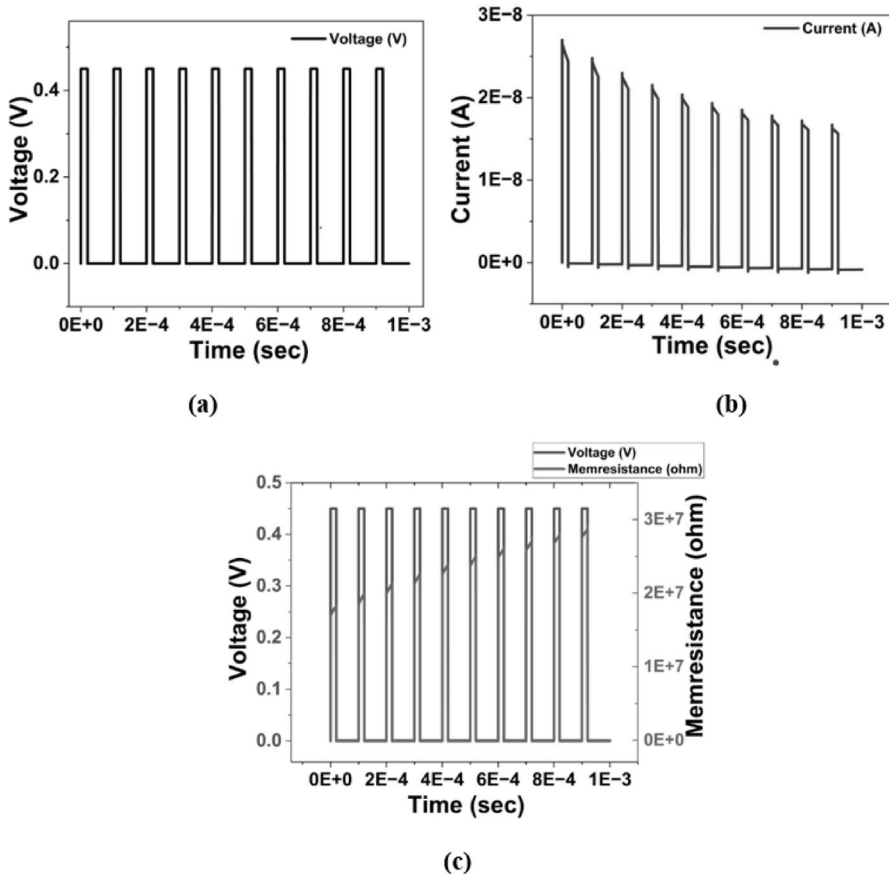


Fig. 8 The non-volatile retention test of proposed memristor emulator while applying the identical write-pulses **a** Digital voltage pulse and **b** as a function of Time (sec), respectively. **c** The variation of memresistance while applying different voltage pulses

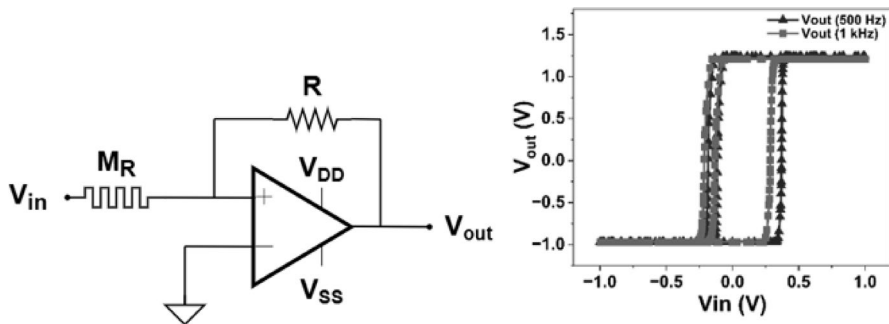


Fig. 9 The schematic of Schmitt trigger implementing proposed memristor emulator, here $R = 1 \text{ k}\Omega$. The output voltage (V_{out}) of proposed Schmitt trigger circuit as a function of input voltage (V_{in}) at the frequencies of 500 Hz and 1 kHz

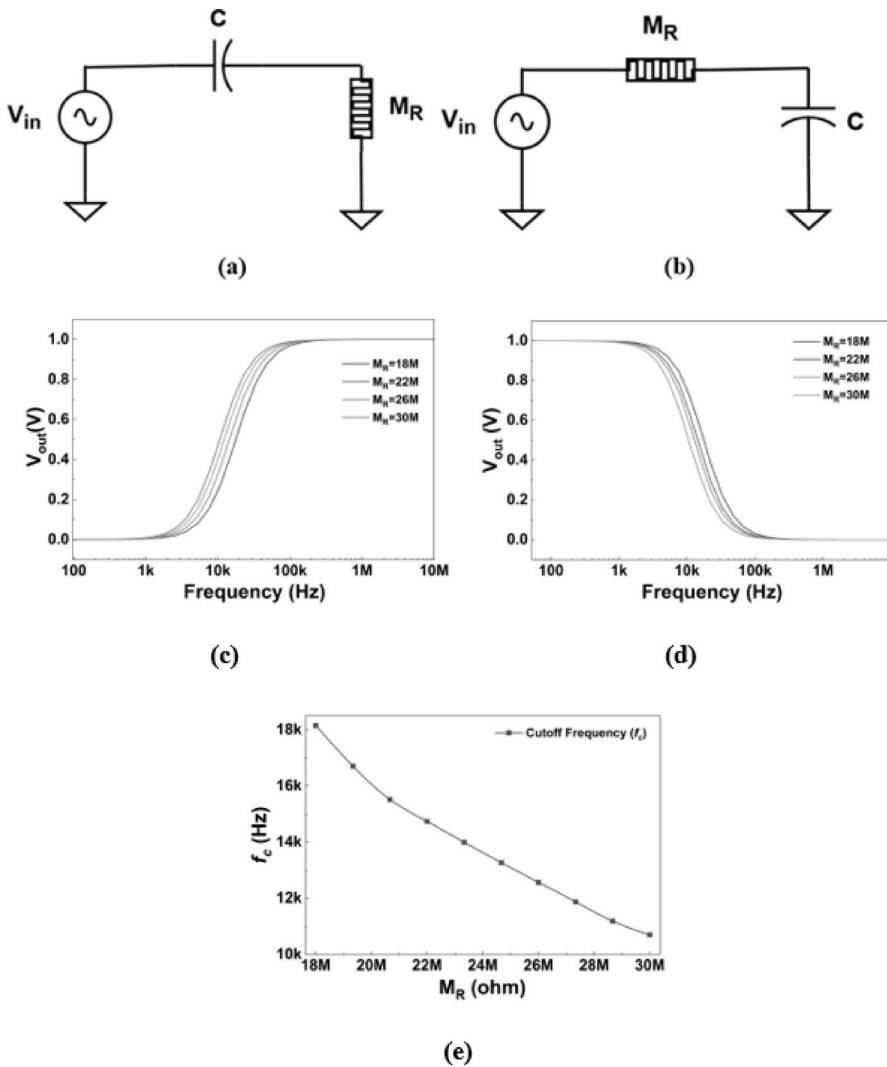


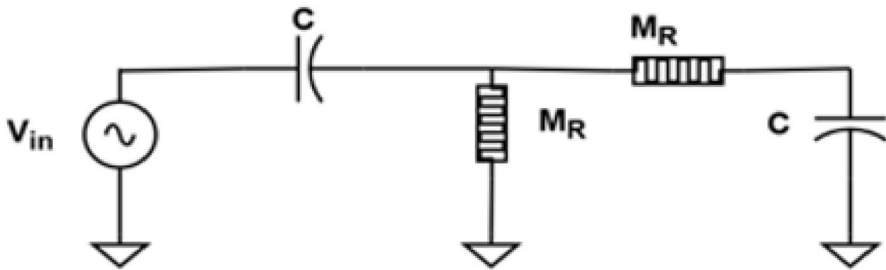
Fig. 10 The schematic of proposed memristor emulator based **a** Low Pass filter **b** High Pass filter circuits utilizing a capacitor of 500 fF. The output voltage as a function of frequency for different memristance (M_R) in **c** and **d** shows the variation in cutoff frequencies for **c** high pass and **d** low pass filter, respectively. **e** The cutoff frequency for both the low and high pass filters decreases with the increase in memristance of the proposed emulator suggesting dynamic changes in filter's time constant

4.3 Bandpass Filter with Dual Thresholds

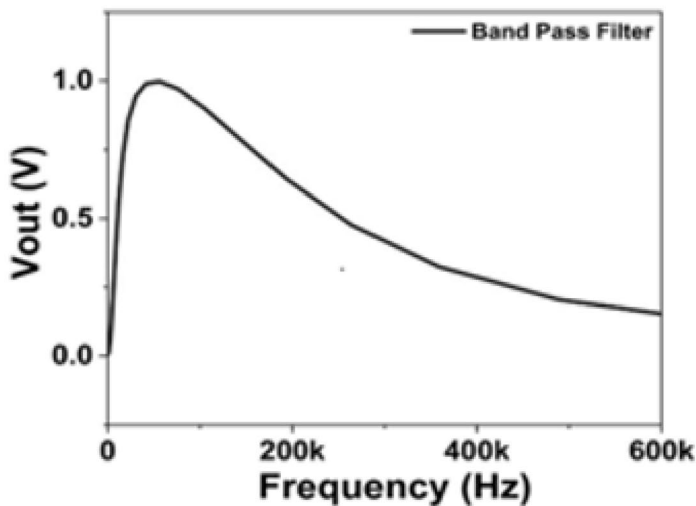
The band-pass response in the Figure 11b rises from 0 V at DC to a peak of ≈ 1 V at the center frequency $f_0 \approx 100$ kHz, then rolls off on either side mirroring the combined action of an HPF and LPF. Using a cascade of two first-order sections (high-pass then low-pass), the overall transfer is

$$H(j\omega) = \frac{j\omega MC}{(1 + j\omega MC)} \frac{1}{(1 + j\omega MC)} \quad (13)$$

yielding a pass-band from about 10 kHz (lower -3 dB corner) up to roughly 400 kHz (upper -3 dB corner). The peak at f_0 corresponds to maximum power transfer where the two RC time constants balance and the filter bandwidth and quality factor are set by the chosen R and C values.



(a)



(b)

Fig. 11 Simulation of Memristor-Capacitor based **a** Band Pass filter circuit at $C=10\text{fF}$ **b** Variation of output voltage with frequency

5 Comparative Study

Table 1 provides a comprehensive comparison of modern memristor emulator circuits, highlighting essential design considerations such as frequency performance, the number of passive components, power supply voltage, grounding configuration, and CMOS process technology. Contemporary designs predominantly include active components like OTAs, CCIIIs, and VDCCs, striving for equilibrium between high-frequency efficacy and circuit simplicity. The configuration using three NMOS transistors and a MOS capacitor demonstrates the most sophisticated frequency response, attaining 50 MHz in a 90 nm GDPK CMOS process, hence signifying its suitability for high-speed analog applications. This design improves the field by utilizing a single NMOS and a MOS capacitor, achieving a frequency of 40 MHz at a low supply voltage of ± 450 mV, while supporting both grounded and floating configurations. These standards signify a significant progression in the creation of high-speed, low-power, and low-complexity memristor emulator designs. Prior techniques operating at lower frequencies, typically around 5 MHz, required an increased quantity of passive components or larger voltage rails, underscoring the inherent trade-offs in circuit design and fabrication technology. The comparison study emphasizes the advantages of modern nanoscale CMOS technology in producing high-performance memristor emulators with minimized component overhead, hence meeting the integration requirements of future neuromorphic and analog computing systems.

6 Conclusion

This article presents a novel circuit design for the floating memristor, employing a single MOSFET and one MOSCAP to fulfill the necessary memristor functionality. The numerical simulation employed 90 nm CMOS technology from GPDK. The characteristics were tested across multiple frequencies, various MOS capacitances, and different temperatures. The suggested memristor emulator operates reliably throughout a frequency range of 500 Hz to 40 MHz, exhibiting a power consumption of 74.724 nW. The execution of the suggested memristor emulator is illustrated using analog computation. The principal benefits of this memristor emulator encompass a reduced number of components, minimal power consumption with 0% static power, and consistent, dependable performance, making it an optimal selection for various applications in computational neuroscience.

Table 1 Comprehensive comparison of modern memristor emulator circuits

Components	Frequency	No. of passive components	Power supply	Floating/grounded	Technology	References
2 OTA	400 kHz	1 C	450 mV	Floating	CMOS	[13]
1 CDBA, 1 OTA	1 MHz	1 C	±900 mV	Both	180 nm CMOS	[14]
1 OTA, 1 VDBA, 1 MOSCAP	5 MHz	–	±900 mV	Both	180 nm CMOS	[15]
1 OTA	1 MHz	1 C	±1 V	Grounded	GDPK 180 nm CMOS	[12]
1 CCII, 1 OTA	30 MHz	–	60 mV	Grounded	TSMC 0.18 μ m	[17]
1 VDCC, 2 PMOS	2 MHz	1 C	±200 mV	Both	TSMC 0.18- μ m	[20]
1 MVDCC	1 MHz	2 R, 1 C	±1 V	Floating	180 nm CMOS	[19]
3 CFOA, 1 Diode	–	3 R, 2 C	±600 mV	Grounded	–	[27]
1 CCII, 1 CCTA	5 MHz	3 R, 1 C	±1.5 V	Floating	TSMC 250 nm	[28]
1 OPAMP, 1 NMOS	20 kHz	3 R, 1 C	±1.5 V	Both	CMOS 90 nm	[30]
3 NMOS, 1 MOSCAP	50 MHz	–	±1.3 V	Floating	GDPK CMOS 90 nm	[31]
1 NMOS, 1 MOSCAP	40 MHz	–	±450 mV	Both	GDPK CMOS 90 nm	This work

Acknowledgements This work is supported by Ministry of Electronics & Information Technology (MeitY), Government of India (GoI) under grant sanction order EE-9/2/2021-R&D-E dated 22.05.2023. Authors acknowledge the use of research facilities developed under DST-FIST Grant SR/FST/ETI-411/2016. KK and MJ acknowledge the financial support under “Visvesvaraya PhD Scheme for Electronics and IT: Phase-II”, MeitY(GoI).

Author Contributions Kunal Kaushik: Formal analysis, Investigation, Methodology, Software, Writing—original draft. Mukul Jangid: Software, Methodology, Formal analysis Gaurav M. Khanal: Data curation, Funding acquisition, Validation, Visualization, Writing—review and editing. Aaishi Dubey: Software, Formal analysis. Sanjeev Kumar: Funding acquisition, Project administration, Writing—review and editing. Satinder K. Sharma: Resources, Supervision, Visualization, Writing—review and editing. Arun K. Singh: Conceptualization, Formal analysis, Funding acquisition, Supervision, Writing—review and editing.

Data Availability All data that support the findings of this study are included within the article.

Declarations

Conflict of interest The authors declare no Conflict of interest.

References

1. M.T. Abuelma'atti, Z.J. Khalifa, A continuous-level memristor emulator and its application in a multi-vibrator circuit. *AEU - Int. J. Electron. Commun.* (2015). <https://doi.org/10.1016/j.aeue.2014.12.011>
2. M.T. Abuelma'atti, Z.J. Khalifa, A new memristor emulator and its application in digital modulation. *Analog Integr. Circ. Sig. Process* **80**(3), 577–584 (2014)
3. K. Bhardwaj, M. Srivastava, Floating memristor and inverse memristor emulation configurations with electronic/resistance controllability. *IET Circuits Devices Syst.* **14**(7), 1065–1076 (2020). <https://doi.org/10.1049/iet-cds.2020.0106>
4. L. Chua, Memristor-the missing circuit element. *IEEE Trans. Circuit Theory* **18**(5), 507–519 (1971). <https://doi.org/10.1109/TCT.1971.1083337>
5. L. Chua, Resistance switching memories are memristors. *Appl. Phys. A* **102**(4), 765–783 (2011). <https://doi.org/10.1007/s00339-011-6264-9>
6. B. Dang, Y. Yu, H. Ma, N. Yang and T. Nyima, A novel charge-controlled memristor model and its emulator circuit, in *2018 IEEE 18th International Conference on Communication Technology (ICCT), Chongqing, China*, 586–590 (2018). <https://doi.org/10.1109/ICCT.2018.8599989>
7. R. Das, S.K. Rai, B. Aggarwal, A floating meminductor emulator using modified differential voltage current conveyor transconductance amplifier and its application. *Analog Integr. Circ. Sig. Process* **119**(3), 475–496 (2024). <https://doi.org/10.1007/s10470-024-02257-0>
8. M. Ghosh, A. Singh, S.S. Borah, J. Vista, A. Ranjan, S. Kumar, MOSFET-based memristor for high-frequency signal processing. *IEEE Trans. Electron Devices* **69**(5), 2248–2255 (2022). <https://doi.org/10.1109/TED.2022.3160940>
9. M. Ghosh, P. Mondal, S.S. Borah, S. Kumar, Resistorless memristor emulators: floating and grounded using OTA and VDBA for high-frequency applications. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **42**(3), 978–986 (2023). <https://doi.org/10.1109/TCAD.2022.3189837>
10. G. Kanyal, P. Kumar, S. Paul, A. Kumar, Ota based high frequency tunable resistorless grounded and floating memristor emulators. *AEU-Int. J. Electron. Commun.* **92**, 124–145 (2018). <https://doi.org/10.1016/j.aeue.2018.05.027>
11. N.A. Khalil, L.A. Said, A.G. Radwan, A.M. Soliman, A simple BJT inverse memristor emulator and its application in chaotic oscillators, in *2019 Fourth International Conference on Advances in Computational Tools for Engineering Applications (ACTEA), Beirut, Lebanon* (2019). <https://doi.org/10.1109/ACTEA.2019.8851104>
12. M.O. Korkmaz, Y. Babacan, A. Yesil, CCII- and OTA-based tunable memcapacitor emulator circuits without using passive elements. *Circuits Syst. Signal Process.* **43**, 4093–4120 (2024). <https://doi.org/10.1007/s00034-024-02681-7>

13. A. Kumar, B. Chaturvedi, A high-quality and space-efficient design for memristor emulation. *Electronics* **13**(16), 3331–3331 (2024). <https://doi.org/10.3390/electronics13163331>
14. K. Kumar, B.C. Nagar, G. Pradhan, Single OTA-based tunable resistorless grounded memristor emulator and its application. *J. Comput. Electron.* (2022). <https://doi.org/10.1007/s10825-022-01955-0>
15. P. Kumar, B.K. Kaushik, R.K. Ranjan, A novel second generation current conveyor (CCII)-based high frequency memristor model. *Microelectron. Eng.* (2023). <https://doi.org/10.1016/j.mee.2023.111938>
16. S. Kvatinsky, E.G. Friedman, A. Kolodny, U.C. Weiser, TEAM: Threshold adaptive memristor model. *IEEE Trans. Circuits Syst. I Regul. Pap.* **60**(1), 211–221 (2013). <https://doi.org/10.1109/TCS.2012.2215714>
17. C. Mead, Neuromorphic electronic systems. *Proc. IEEE* **78**(10), 1629–1636 (1990). <https://doi.org/10.1109/5.58356>
18. L. Minati, A chaotic circuit based on a physical memristor. *Chaos Solitons Fractals* **138**, 109990–109990 (2020). <https://doi.org/10.1016/j.chaos.2020.109990>
19. M. Korkmaz, Y. Babacan, A. Yeşil, A new ccii based meminductor emulator circuit and its experimental results. *AEU-Int. J. Electron. Commun.* **158**, 154450 (2023). <https://doi.org/10.1016/j.aeue.2022.154450>
20. V. Ntinis, A. Ascoli, Toward simplified physics-based memristor modeling of valence change mechanism devices. *IEEE Trans. Circuits Syst. II Express Briefs* **69**(5), 2473–2477 (2022). <https://doi.org/10.1109/TCSII.2022.3160304>
21. I. Pal, V. Kumar, N. Aishwarya, A. Nayak, A. Islam, A vdtta-based robust electronically tunable memristor emulator circuit. *Analog Integr. Circ. Sig. Process* **104**(1), 47–59 (2019). <https://doi.org/10.1007/s10470-019-01575-y>
22. A.Y. R., N. Raj, G. Trivedi, A MOS-DTMOS implementation of floating memristor emulator for high-frequency applications. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **31**(3), 355–368 (2023). <https://doi.org/10.1109/TVLSI.2022.3227201>
23. R. Ranjan, S. Prasad, S. Roushan, B. Kumari, N. Rani, F. Khateb, High-frequency floating memristor emulator and its experimental results. *IET Circuits Devices Syst.* **13**(3), 292–302 (2019). <https://doi.org/10.1049/iet-cds.2018.5191>
24. D.B. Strukov, R.S. Williams, Exponential ionic drift: fast switching and low volatility of thin-film memristors. *Appl. Phys. A* **94**(3), 515–519 (2008). <https://doi.org/10.1007/s00339-008-4975-3>
25. D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, The missing memristor found. *Nature* **453**(7191), 80–83 (2008). <https://doi.org/10.1038/nature06932>
26. B. Suresha, C. Shankar, S.B. Rudraswamy, A floating memristor emulator for analog and digital applications with experimental results. *Analog Integr. Circ. Sig. Process* **118**(1), 77–90 (2023). <https://doi.org/10.1007/s10470-023-02221-4>
27. S. Tasneem, P. Sharma, R. Ranjan, F. Khateb, Electronically tunable memristor emulator implemented using a single active element and its application in adaptive learning. *Sensors* **23**(3), 1620 (2023). <https://doi.org/10.3390/s23031620>
28. D. Vaidya, S. Kothari, T. Abbey, S. Stathopoulos, L. Michalas, A. Serb, T. Prodromakis, Compact modeling of the switching dynamics and temperature dependencies in TiO_x memristors—Part II: physics-based model. *IEEE Trans. Elect. Devices* **68**(10), 4885–4890 (2021). <https://doi.org/10.1109/TEDE.2021.3102002>
29. J. Vista, A. Ranjan, Flux controlled floating memristor employing VDTA: incremental or decremental operation. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **40**(2), 364–372 (2020). <https://doi.org/10.1109/TCAD.2020.2999919>
30. N. Yadav, S.K. Rai, R. Pandey, New grounded and floating memristor emulators using OTA and CDBA. *Int. J. Circ. Theory Appl.* **48**(7), 1154–1179 (2020). <https://doi.org/10.1002/cta.2774>
31. S. Yang, B. Liu, L. Wei, D. Wu, Y. He, G. Dai, Design and application of passive very high-frequency memristor emulator. *Circuits Syst. Signal Process.* **44**(4), 2330–2348 (2024). <https://doi.org/10.1007/s00034-024-02956-z>
32. A. Yesil, Y. Babacan, F. Kacar, Electronically tunable memristor based on VDCC. *AEU - Int. J. Electron. Commun.* **107**, 282–290 (2019). <https://doi.org/10.1016/j.aeue.2019.05.038>
33. D. Yu, T. Sun, C. Zheng, H. Iu, T. Fernando, A simpler memristor emulator based on varactor diode. *Chin. Phys. Lett.* **35**(5), 058401 (2018). <https://doi.org/10.1088/0256-307x/35/5/058401>
34. M.Z. Hosbas, F. Kaçar, A. Yesil, Memcapacitor emulator using VDTA-memristor. *Analog Integr. Circ. Sig. Process* **110**, 361–370 (2022). <https://doi.org/10.1007/s10470-021-01974-0>

35. D. Ielmini, V. Milo, Physics-based modeling approaches of resistive switching devices for memory and in-memory computing applications. *J. Comput. Electron.* **16**, 1121–1143 (2017). <https://doi.org/10.1007/s10825-017-1101-9>

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Springer Nature or its licensor (e.g. a society or other partner) holds exclusive rights to this article under a publishing agreement with the author(s) or other rightsholder(s); author self-archiving of the accepted manuscript version of this article is solely governed by the terms of such publishing agreement and applicable law.

Authors and Affiliations

Kunal Kaushik¹ · Mukul Jangid¹ · Gaurav M. Khanal² · Aaishi Dubey¹ · Sanjeev Kumar³ · Satinder K. Sharma⁴ · Arun K. Singh¹ 

✉ Arun K. Singh
arun@pec.edu.in

Kunal Kaushik
masterkkaushik1999@gmail.com

Mukul Jangid
mukuljangid777@gmail.com

Gaurav M. Khanal
gauravmanikhanal@gmail.com

Aaishi Dubey
aaishidubey@pec.edu.in

Sanjeev Kumar
sanjeev@pec.edu.in

Satinder K. Sharma
satinder@iitmandi.ac.in

¹ Semiconductor Research Centre, Department of Electronics and Communication Engineering, Punjab Engineering College (Deemed to be University), Chandigarh, India

² Department of Electrical and Electronics Engineering, J K Lakshmi Pat University, Jaipur, Rajasthan, India

³ Department of Physics, Punjab Engineering College (Deemed to be University), Chandigarh, India

⁴ School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT), Mandi, Himachal Pradesh, India